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Thermo-mechanical Reliability of 3-D Interconnects Containing Through-Silicon-Vias (TSVs)

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Thermo-mechanical Reliability of 3-D Interconnects Containing Through-Silicon-Vias (TSVs)

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Dedication

To my beloved parents and

Chan Master, Wu Jue Miao Tian

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Thermo-mechanical Reliability of 3-D Interconnects Containing Through-Silicon-Vias (TSVs)

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This dissertation focuses on one of the most active research areas in the microelectronics industry: Thermo-mechanical reliability of 3-D interconnects containing through-silicon-vias (TSVs). This study constitutes two parts: 1. Thermal stress measurement on TSVs; 2. Analyses on thermo-mechanical reliability of TSVs. In the first part, a metrology for stress measurement of through-silicon-via (TSV) structures was developed using a bending beam technique. The bending curvature induced by the thermal expansion of a periodic array of Cu TSVs was measured during thermal cycles. The stress components in TSV structures were deduced combining the curvature measurement with a finite-element-analysis (FEA). Temperature-dependent thermal stresses in Cu TSVs and in Si matrix were derived.

In the second part, the reliability issues induced by the thermal stresses of TSVs were analyzed from several aspects, including the carrier mobility change in transistors, the interfacial delamination of TSVs, and thermal stress interactions between TSVs. Among them, the mobility change in transistors was found to be sensitive to the normal

stresses near the Si wafer surface. The surface area of a high mobility change was defined as the keep-out zone (KOZ) for transistors. FEA simulations were carried out to calculate the area of KOZ surrounding TSVs. The area of KOZ was found to be mainly determined by the channel direction of the transistor as a result of anisotropic piezoresistivity effects. FEA simulations also showed that the KOZ can be controlled by TSV geometry, material selection, etc.

Interfacial delamination of TSVs was found to be mainly driven by a shear stress concentration at the TSV/Si interface. Crack driving force for TSV delamination was calculated using FEA simulations, which take into account the magnitude of thermal load, TSV geometry, TSV materials, etc. The results provided a design guideline to improve the TSV delamination problem.

In the last, the stress interaction among TSV arrays was examined using a bi-TSV model. In the Cartesian coordinate system, thermal stresses can be intensified or suppressed between TSVs, depending on how TSVs are located. Further analyses suggested that the area of KOZ and the TSV-induced Si cracking can both be improved by optimizing the arrangement of the TSV arrays.

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Chapter 1: Introduction

In the past three decades, the microelectronics industry has largely been driven by Moore's law to continuously increase device density and circuit speed. This has led to miniaturization of the dimensions of semiconductor devices from 10 μm to 32 nm in the current technology generation. To sustain this trend, major technology and economical barriers are to be expected for future device manufacturing, especially at a scale below ~10 nm. To drive Moore's law forward, the microelectronics industry is looking for technical solutions by innovative system integration other than simply to continue down-scaling of microelectronic devices on a 2-dimentional plane. Concurrently, there is an escalating demand to minimize the dimension of electronic packages, particularly for consumer electronic products such as mobile devices. These technological needs have stimulated great interest to develop innovative approaches such as 3-dimentional (3-D) integration technology, where multiple IC chips of different functionality can be integrated into a single and compact electronic package. Such a 3-D integrated system is schematically shown in Figure 1.1, where several classes of IC chips are stacked in the vertical direction. In this way, the 3-D integration can achieve a high circuit density and performance through a heterogeneous integration of multiple IC chips.

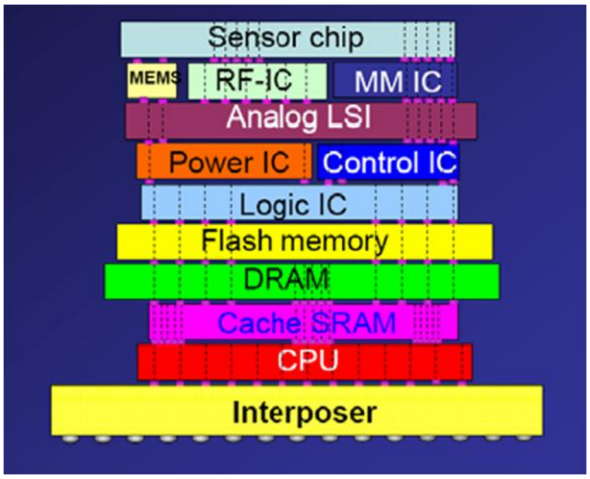


Figure 1.1: Schematic diagram showing the 3-D integration of multiple IC chips of different functionalities. (Source: Zycube in Ref. [1])

To enable the 3-D integration, through-silicon-vias (TSVs) are embedded into the silicon substrate to form vertical, electrical connections between stacked IC chips. Nevertheless, a myriad of reliability concerns have arisen when TSVs are implemented. Among them, thermal stresses induced by the thermal expansion mismatch between Si and TSVs pose one of the severest challenges to the reliability of 3-D ICs. Intensive investigation has been carried out to study the thermal stress in the TSV infrastructures because it was found to cause fractures in the back-end-of-line (BEOL) interconnects. Furthermore, thermal stresses can alter the carrier mobility in the transistors, causing malfunction in the electrical circuits.

This dissertation focuses on one of the most active research areas in the microelectronics industry: Thermo-mechanical reliability of 3-D interconnects. There are two objectives in this study. First, a metrology for stress measurement of TSV structures is developed using a Bending Beam (BB) technique. The bending curvature induced by the thermal expansion of Cu TSVs is measured during thermal cycles. The stress components in TSV structures are further deduced, combining the curvature

measurement with finite-element-analysis (FEA). This metrology is demonstrated by measuring the thermal stresses generated in a periodic array of Cu TSVs embedded in Si during thermal cycling. The experimental procedure and the FEA developed will be described in Chapter two.

The second objective is to investigate the reliability issues induced by the thermal stresses of TSVs from several aspects, including the impact on carrier mobility in transistors, the interfacial delamination of TSVs, and cracking of Si substrates. Analytical solutions and FEA simulations are employed to quantify aforementioned risks. These analyses are described in Chapter three through Chapter five.

1.1 ADVANTAGES OF 3-D INTEGRATION

3-D integration is expected to bring significant benefits when compared to the existing 2-D integrated structure. Major advantages of 3-D integration include: (a) better electrical performance; (b) lower power consumption; (c) higher device density and smaller packaging form factor [2]. The advantages (a) and (b) can be interpreted from a conceptual illustration, as shown in Figure 1.2. In Figure 1.2a, two IC chips (logic and memory) are connected to each other using current 2-D interconnects. Wires that connect between chips can be as long as the lateral dimension of chips, i.e. a length of centimeter-scale. The logic chip has to wait for a relatively long time for a memory access to complete before it can process the data, causing a signal delay that degrades the electrical performance. This is also known as the memory latency. In Figure 1.2b, two IC chips are connected vertically using 3-D interconnects with TSVs. The wiring distance between two chips, if properly designed, can be as short as the vertical dimension between the

chips, i.e. a length of micron-scale. Consequently, 3-D infrastructures can significantly reduce the memory latency and hence improve the chip performance.

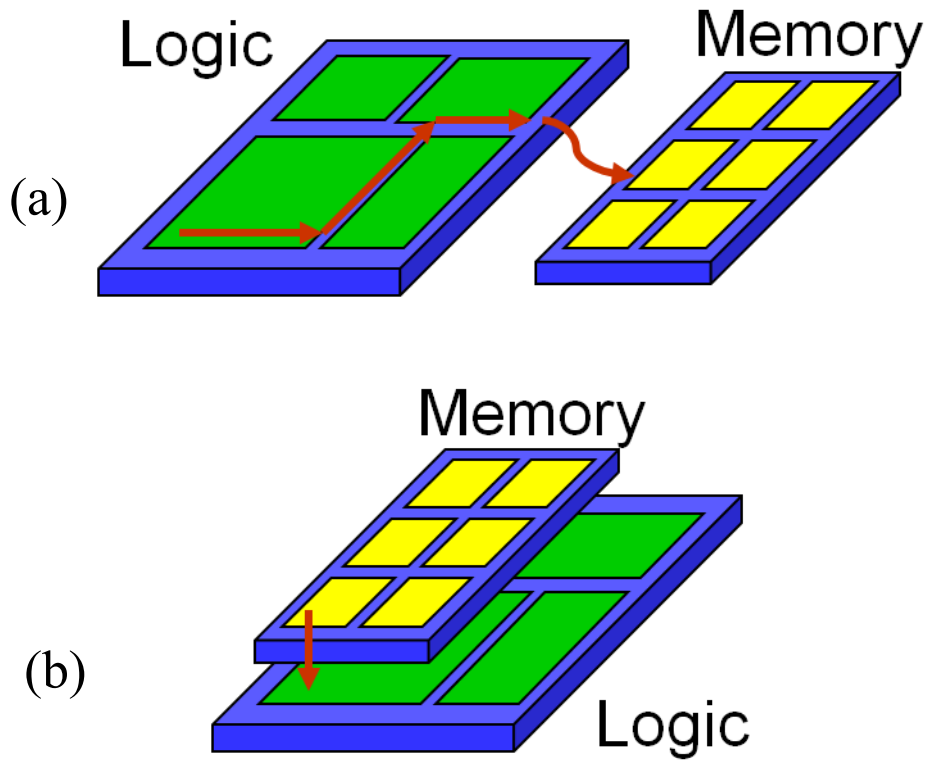


Figure 1.2: Schematic diagrams showing the difference between 2-D and 3-D interconnects: (a) logic and memory chips are connected horizontally using existing 2-D approach; (b) logic and memory chips are connected vertically using 3-D interconnects. (Source: Beyne in Ref. [1]; this diagram is redrawn by the author)

Data transmission along interconnect wires consume a significant portion of electrical power. Therefore, having shorter interconnects between stacked IC chips can reduce the power use [2][3]. A previous study indicates that, by partitioning a given

circuit into multiple strata, the interconnect power consumption decreased roughly with the square root of the number of strata (Figure 1.3) [3]. This is due to a shorter interconnect length in the multi-strata circuit.

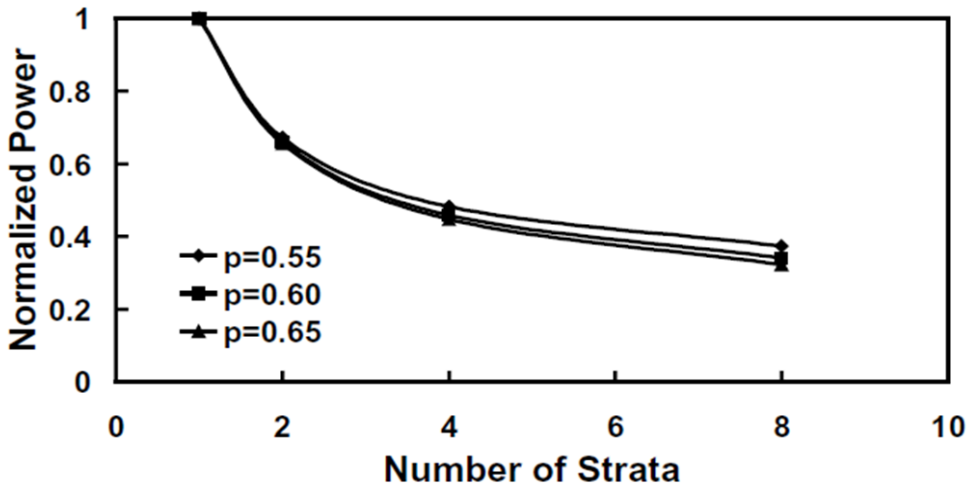


Figure 1.3: Projected interconnect power consumption as a function of the total number of partitioned strata for a given circuit. *P* stands for the Rent's exponent. (Source: Joyner in Ref. [3])

The other benefit of 3-D integration is to increase the device density while to reduce the package form factor. The advantage of device density/package form factor can be readily demonstrated using an example of stacked die memory. Figure 1.4 demonstrates a 16 GB NAND flash memory consisting of 8 strata of stacked dies. Each die has been thinned down to a thickness of 50 μm, and then are vertically interconnected using TSVs. Compared to an equivalent product without TSV interconnects, such stacking structure yields a 30% thinner package thickness along with a 15% smaller footprint [2]. Therefore, 3-D integrated memory has a tremendous potential for mobile communication devices since it enables massive data storage in a more limited space.

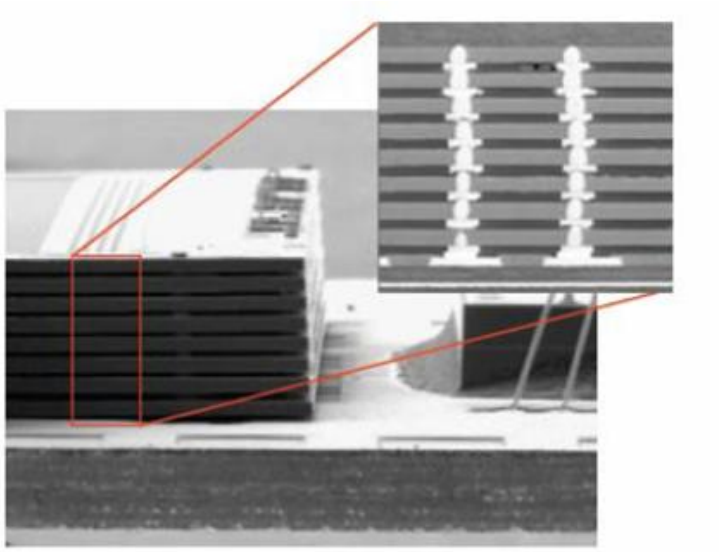


Figure 1.4: Samsung 16 GB NAND flash memory consisting eight 50-μm thick chips. (Source: Samsung in Ref. [2])

1.2 MANUFACTURING PROCESSES FOR 3-D INTERCONNECTS

To enable the 3-D integration, three major types of manufacturing technologies are required [4], including: (a) formation of TSVs, (b) Si wafer thinning and handling, and (c) wafer alignment and bonding. The formation of TSVs can occur either before or after the wafer/die bonding process. The terms "via-first process" and "via-last process" are used to describe the sequence of TSV formation relative to the wafer/die thinning and bonding processes. Within the context of the subjects discussed in this dissertation, the "via-first" manufacturing processes for TSVs are explained as below. Figure 1.5a shows a schematic drawing of a via-first BEOL TSV, which is fabricated in a sequence between the completion of the front-end-of-lrine (FEOL) devices and the early stage of BEOL processes [5]. Figure 1.5b illustrates a simplified manufacturing process flow for this type of TSV.

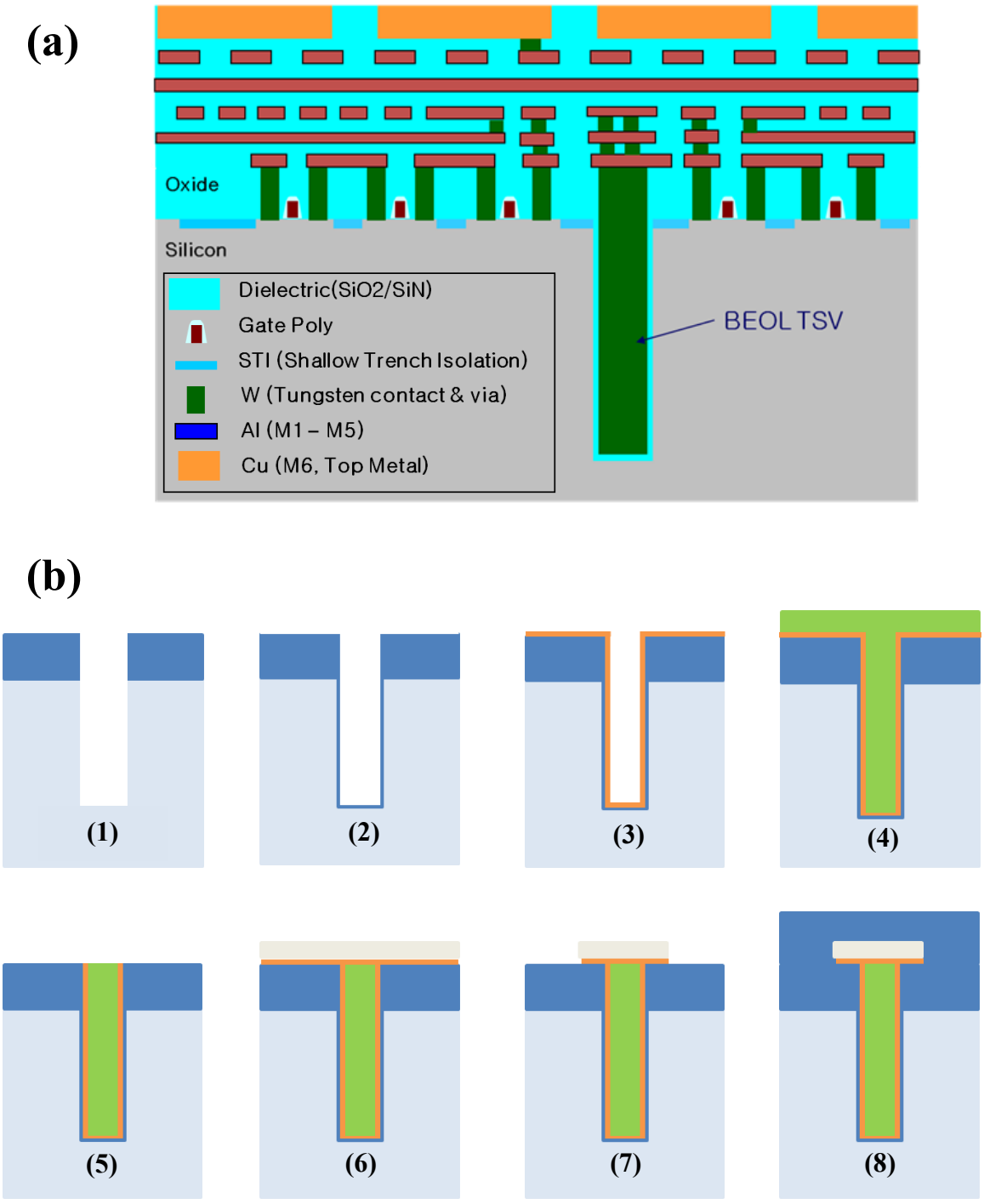


Figure 1.5: (a) Illustration of a BEOL TSV embedded in a Si wafer (Source: Tezzaron in Ref. [5]); (b) A simplified manufacturing process flow for a BEOL TSV.

The process flow to form a BEOL TSV (Figure 1.5b) is described in sequence as following:

(1). Via opening:

After the completion of FEOL devices, blind via holes are opened in selected locations on the Si wafer. There are two types of via opening methods: (a) deep reactive ion etching (DRIE), also known as the "Bosch process" and (b) laser drilling. Depending on the design and applications, the diameter of BEOL TSVs can range from a few microns to ~10 μm. The depth of via hole is roughly the same as the targeted wafer thickness for stacking, which is ~50 μm for memory stacks and ~25 μm for a microprocessor [1].

(2). Deposition of dielectric liner:

Before filling the via holes with metallic materials, a conformal dielectric liner is deposited on the via sidewalls and the via bottom. In general, silicon dioxide is selected as the dielectric material to insulate the via from the Si substrate. This silicon dioxide layer (normally below 1 μm in thickness) is deposited using a plasma-enhanced chemical vapor deposition (PECVD) process at ~300^{o}C. TEOS (tetraethyl-orthosilicate) is commonly used as the silicon source in such a PECVD process [6].

Polymeric dielectric materials such as benzocyclobutene (BCB) or parylene have also been developed as the sidewall insulators for TSVs of a larger diameter (~100 μm) and of a lower depth-to-diameter aspect ratio [7][8]. Polymer dielectric materials can be spin-coated or spray-coated on TSV sidewalls [9], with a thickness of a few microns. The advantages of the polymeric liner include a lower process temperature and a lower dielectric constant than silicon dioxide.

(3). Deposition of diffusion barrier/adhesion layer:

After deposition of the dielectric liner, a thin layer of diffusion barrier is often deposited on the via sidewalls for Cu TSVs using a CVD process. The barrier layer is usually made of metallic materials such as Ti, Ta, and their respective nitrides, TiN and TaN, with thickness of about 50 nm [10]. Such barriers prevent Cu contamination of the Si substrate. In addition, Ta/TaN thin films promote the interfacial adhesion between Cu material to the Si substrate, and hence improve the reliability of TSV [11].

(4). TSV filling:

Cu and W are the most commonly used materials for metallization of TSV. Cu can be deposited using either a CVD process or an electroplating process. The CVD Cu process can fill via holes up to ~3 μm in diameter with high aspect ratios, while electroplating of Cu can fill via holes larger than ~5 μm in diameter [12]. For electroplated Cu TSVs, a conformal layer of Cu seed layer is deposited on via sidewalls/via bottom before the electroplating process [13]. Because of the high aspect ratio of the via holes, additional process developments are required in order to achieve a bottom-up, void-free Cu filling [14]. For W TSVs, a CVD process at ~450^{o}C is generally used. Limited by the high residual stress after deposition, CVD W can only fill via holes with a diameter (or lateral width) of up to ~3 μm [12].

(5~8). Metal pad formation for subsequent BEOLs :

After filling the TSV, the metal overburden on the top wafer surface is removed by either a reactive ion etching (RIE) or a chemical-mechanical polishing (CMP) process.

This is followed by deposition of an overlaying metal pad on top of the TSV to form interconnects to the subsequent BEOL structures.

1.3 THERMO-MECHANICAL RELIABILITY CONCERNS

During subsequent BEOL and die-stacking processes, Si wafers containing TSVs are subjected to repeated thermal loadings. Due to the mismatch in thermal expansion coefficients (CTEs) between the TSV materials and the Si substrate, thermal stresses can develop in the interconnect structures, raising thermo-mechanical reliability concerns.

One of the reliability concerns is the stress-induced resistance change in transistors. Here a simplified risk assessment is given below. Consider an isolated Cu TSV in Si subjected to a thermal load $\Delta T = 100^{o}C$. The maximum radial stress σ_r in the Si can be approximated using a 2-D analytic solution [15]:

$$\sigma_r^{Si} = \frac{-B\Delta\alpha\Delta T}{2}, \qquad (1.1)$$

Where B is the biaxial modulus of Si (180 GPa), and $\Delta\alpha$ is the CTE mismatch between Cu and Si (14.7 ppm/^{o}C). According to Equation 1.1, the maximum radial stress in Si is -132 MPa. It has been reported that a stress of 100 MPa can induce up to 7% of resistance change in a p- channel transistor [16]. Consequently, the 100^{o}C thermal load can induce up to -9% of resistance change close to the edge of a TSV. To ensure proper functionality of the transistors, it is necessary to keep the transistors away from the surface area of high stresses surrounding a TSV. Such area is also known as the keep-out zone (KOZ). In Chapter 3, the near-surface thermal stresses will be investigated followed by a study on KOZ for p- and n- channel devices.

Another reliability concern is the TSV extrusion (or TSV pumping) problem. During TSV manufacturing processes, Cu TSVs were found to extrude out of the Si wafer surface, causing fracture of the overlaying dielectric material (silicon oxide). Such extrusion phenomenon is illustrated in Figure 1.6a, and a failure analysis image is shown in Figure 1.6b.

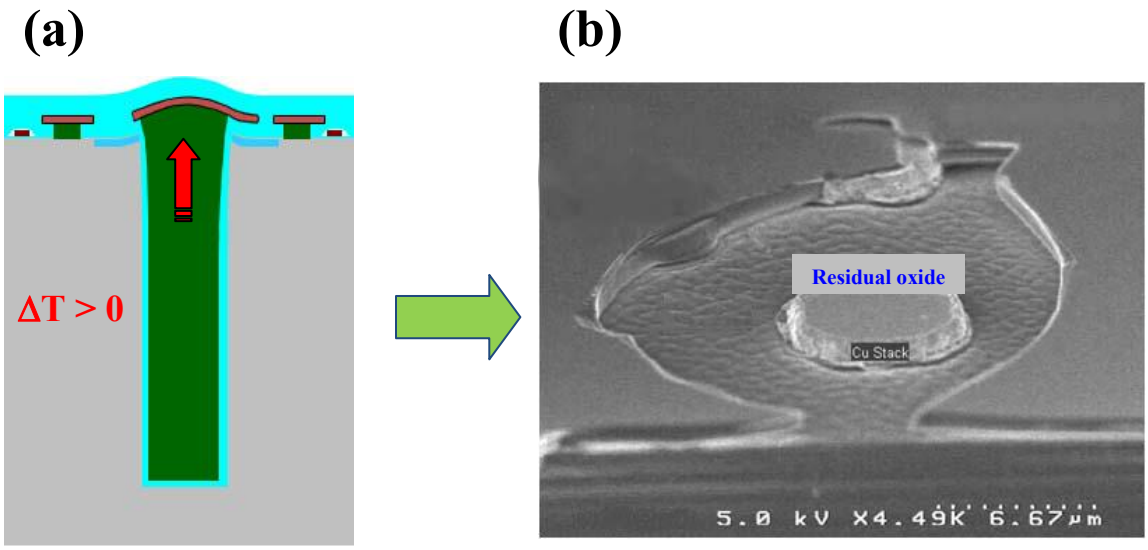


Figure 1.6: (a) Illustration of TSV extrusion under a positive thermal loading; (b) fracture of the dielectric layer induced by the extrusion of TSV underneath (Source: Tezzaron in Ref. [17]).

Before a TSV can extrude to cause the fracture damage, the vertical, circumferential interface between the TSV and the Si matrix must already be delaminated. The interfacial delamination is found to be driven by the shear stress concentration at the edge of the TSV near the wafer surface. This TSV delamination or extrusion problem will be examined in Chapter 4.

1.4 OBJECTIVE AND APPROACH

The objectives of this work are: (1) To establish a stress measurement technique for TSV structures, and (2) To investigate potential failure modes of 3-D/TSV structures. The key contributions of this dissertation are as follows:

Bending beam technique for stress measurement on TSVs

In this dissertation, a metrology for stress measurement of TSV structures based on the bending beam technique is developed. In a TSV structure, for example, a Cu TSV embedded in a Si substrate, a complete stress analysis will require information on the stress characteristics for both Cu and Si. In this study, a curvature measurement is performed on annular Cu TSV arrays under repeated thermal cycles. The change in the beam curvature during thermal cycles provides a measure of the average thermal stress in the composite TSV structure. FEA simulations are performed to correlate the beam curvature to the stress components in the TSV test structure. Combining the curvature measurement and the FEA analysis, the thermal stresses in the annular Cu TSV structure are derived. This method is complimentary to the micro Raman technique which determines the stress distribution in the Si near the TSV by measuring the frequency shift of the Raman peak of Si. Together these two techniques provide the information required to understand the stress behavior of the composite TSV structure. The bending beam method is demonstrated in Chapter 2.

Quantitative thermo-mechanical reliability analyses

Potential thermo-mechanical failure modes of 3-D/TSV structures are examined, including the effects of thermal stresses on the electrical performance of devices, on the interfacial delamination, and on the cracking in silicon matrix. Analytical solutions and

FEA simulations are carried out to quantitatively assess the driving forces of aforementioned reliability issues. Chapter 3 analyzes the thermal stress in the Si substrate and its effect on the electrical performance of the device. In Chapter 4, the thermal stresses near the TSV/Si interface are investigated, and the crack driving force for TSV delamination is calculated for various TSV structures and materials. A TSV protrusion mechanism is proposed in Chapter 4 based on the driving force calculations. In Chapter 5, the proximity effect of multiple TSVs is discussed. According to the discussion from Chapter 3 through Chapter 5, methods to improve the thermo-mechanical reliability of 3-D interconnects are summarized in Chapter 6.

Chapter 2: Thermal Stress Measurement on TSVs using Bending Beam Technique

2.1 INTRODUCTION

In 3-D ICs, the through-silicon-via (TSV) is a critical element connecting die-to-die in the integrated stack structure. The thermal expansion mismatch of the TSV with Si can induce sufficient stresses to drive interfacial crack growth and degrade device performance in 3-D ICs [18][19]. This raises serious reliability concerns and has stimulated great interests from the semiconductor industry to investigate the thermal stress characteristics and their impact on the structural reliability of TSV structures. The stress state of TSV is highly complex 3-D due to its high-aspect ratio and the design of the 3-D stack structure. To study the thermal stress characteristics, it is important to understand the nature of the thermal stresses and their dependence on the material, configuration, and processing of the TSV structures. There are two general approaches to investigate the thermal stress characteristics, one based on analytical methods or modeling simulation and the other by experimental measurements. These are truly complimentary techniques in that the modeling simulation requires knowledge of material properties which have to be measured and the results have to be verified by experiments. Similarly, experiments are commonly performed on test structures designed for specific techniques where the results have to be extracted by stress analysis or simulation.

Several experimental techniques have been developed for on-wafer stress measurement. These include the wafer bending technique which can be used to measure the in-plane stress of a thin film by tracking the bending curvature of the Si wafer underneath [20]. X-ray diffraction is a technique which measures the elastic strains in poly-crystalline metallic films or line structures by measuring the lattice parameter

change during thermal cycling [21]. Raman spectroscopy [22] is another technique which measures the sum of the in-plane stresses on a Si wafer by monitoring the frequency shift of the Raman peaks induced by fabrication or thermal process, such as ion implantation. Recently, the Raman and the X-ray diffraction techniques have been developed for stress measurement for TSV structures in 3-D integration [18][23]. These techniques measure only the combination of certain stress components induced by TSVs. For example, the micro-Raman technique has demonstrated its capability in measurement of the stress distribution in Si around a Cu TSV with a sub-micron spatial resolution. The result yielded only a combination of the in-plane near-surface stress components in Si. To extract individual stress components, finite-element-analysis (FEA) is required [18][23].

In this chapter, a metrology is developed for stress measurement of TSV structures based on the bending beam technique in combination with FEA. The technique first measures the bending curvature of a test structure containing periodic blind TSVs using a laser deflection system. The change in the beam curvature during thermal cycling provides a measure of the average thermal stress in the composite TSV structure. Then FEA simulations are performed to correlate the beam curvature to the stress components in the TSV test structure. The results show that the stress components in the annular vias are linearly dependent on the bending curvature of the Si beams. Finally, the thermal stresses in the annular TSV structure are derived by combining the curvature measurement and the FEA analysis.

2.2 BENDING BEAM EXPERIMENT

2.2.1 Curvature measurement using bending beam system

In this section, the bending beam technique for thermal stress measurement is introduced. The bending beam system employs an optical method to monitor the curvature of TSV specimens with respect to temperature. Here only the experimental procedures are explained while the analysis to deduce the thermal stresses in the TSV test structure is described later in Section 2.3.

The bending beam system consists of a laser-positioning system, a vacuum chamber with environmental temperature control, and a controlling personal computer. A schematic setup of the bending beam system is shown in Figure 2.1.

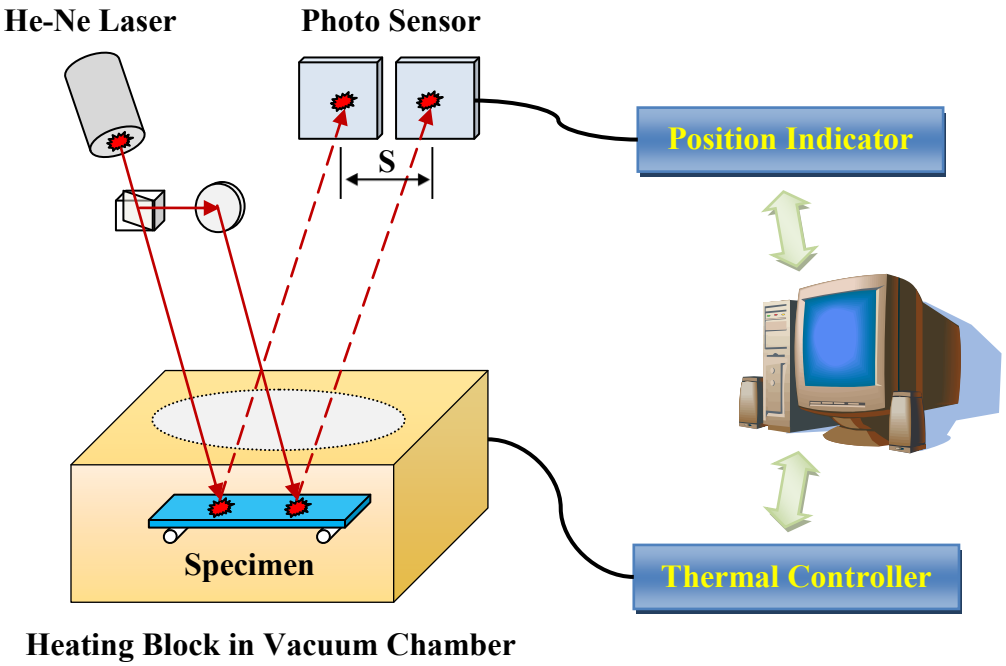


Figure 2.1: Schematic setup of the bending beam system.

As illustrated in Figure 2.1, specimens of a strip shape are placed on a heating stage in the vacuum chamber. To measure the bending curvature of the specimen, the He-Ne laser beam is split into two parts with each impinging on the surface of the specimen through a transparent viewing window, and then the positions of the reflected laser beams are tracked using two photo sensors. The distance between the two laser spots on photo sensors, S, is measured using a position indicator. The bending curvature, κ, can be expressed as below [24]:

$$\kappa - \kappa_o = \frac{1}{R} - \frac{1}{R_o} = \frac{S_o - S}{2DL}, \tag{2.1}$$

where R is the radius of curvature, D is the distance between the two laser spots on the specimen, and L is the distance between the specimen and photo sensors. The subscript "o" stands for the baselines of a reference state. The spatial relationships among these parameters are illustrated in Figure 2.2.

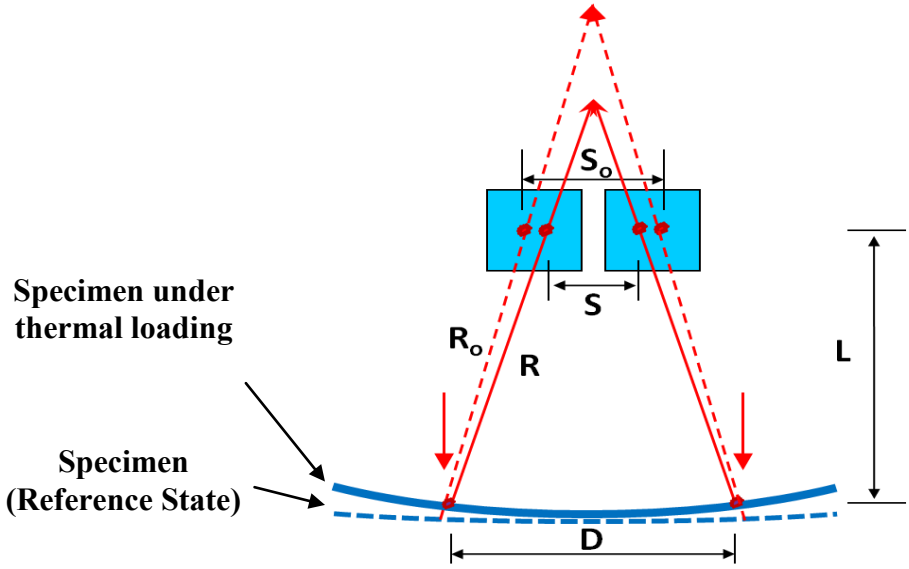


Figure 2.2: Spatial relationships among parameters in Equation 2.1.

2.2.2 Bending beam specimen: annular Cu via array in Si

Si wafers containing periodic arrays of blind annular Cu TSVs were co-designed by UT/siXis (Morrisville, NC) and fabricated by SVTC (Austin, TX) for bending beam measurement. To fabricate the annular vias, a square grid array of circular areas (90 μm in diameter) is first photo-patterned on (001) Si wafers, and then a Bosch Si etching process is performed to drill circular holes to form periodic blind vias in the Si wafer. After the Si etching process, a conformal coating of dielectric material (~ 2 μm thick silicon oxide) is deposited on the wafer surface and at the via sidewall. Finally, the wafers are electroplated with a thin layer of Cu ~ 2 μm in thickness to form annular Cu vias. A schematic of the cross section view of the via test structure after electroplating is illustrated in Figure 2.3.

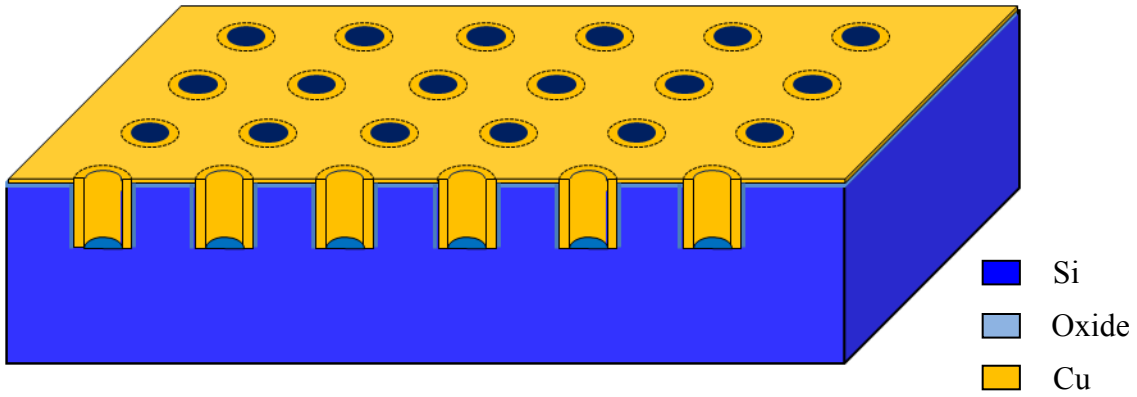


Figure 2.3: Cross-sectional view of the TSV test structure containing annular Cu vias (gold) in a Si substrate (blue).

The samples used for bending beam measurements were diced from the Si wafer into 4 mm-by-40 mm strips. In order to measure the thickness of Cu on the via sidewall, the bending beam specimens were polished on the edge to expose the cross-section of a

row of TSVs. The polished specimen was examined using a SEM/EDS system (JEOL JSM-5610). A cross-section SEM image of the annular via array is shown in Figure 2.3.

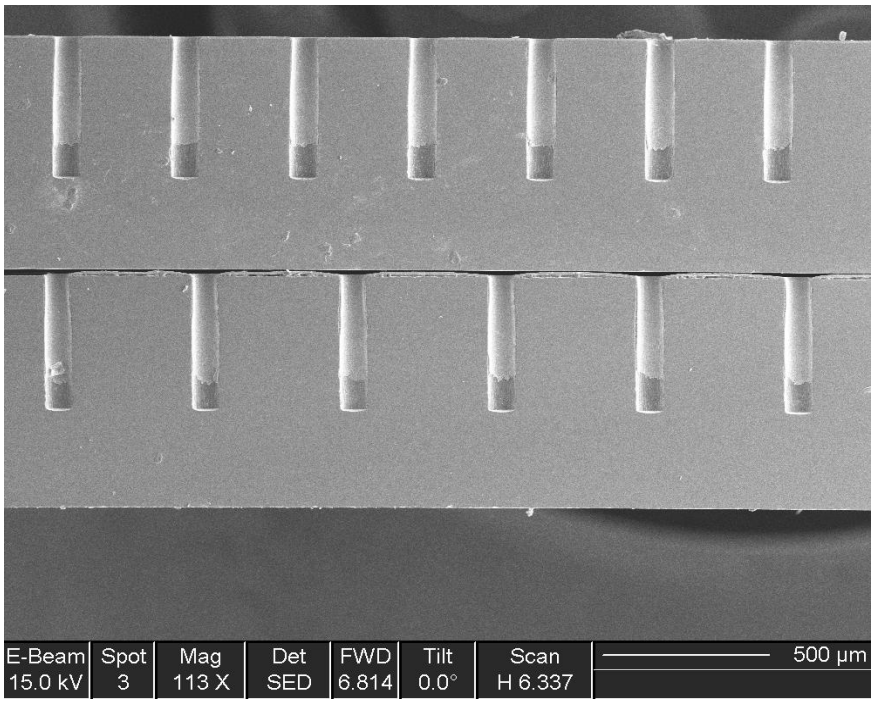


Figure 2.3: Cross-section image of bending beam specimen.

The electroplated annular Cu layer does not cover the whole length of the via sidewalls, as shown by the Cu element mapping using EDS in Figure 2.4. The x-ray element analysis shows that the electroplated Cu film covers about two thirds of the via sidewall extending from the top wafer surface to the lower portion of vias. The reason that Cu is not electroplated to the via bottom can be attributed to the non-uniformity of the Cu seed layer on the via sidewall. The non-uniformity of the Cu seed layer is most probably due to the high aspect ratio of the via, making it difficult for Cu to be deposited on the bottom of the via holes using a PVD sputtering process.

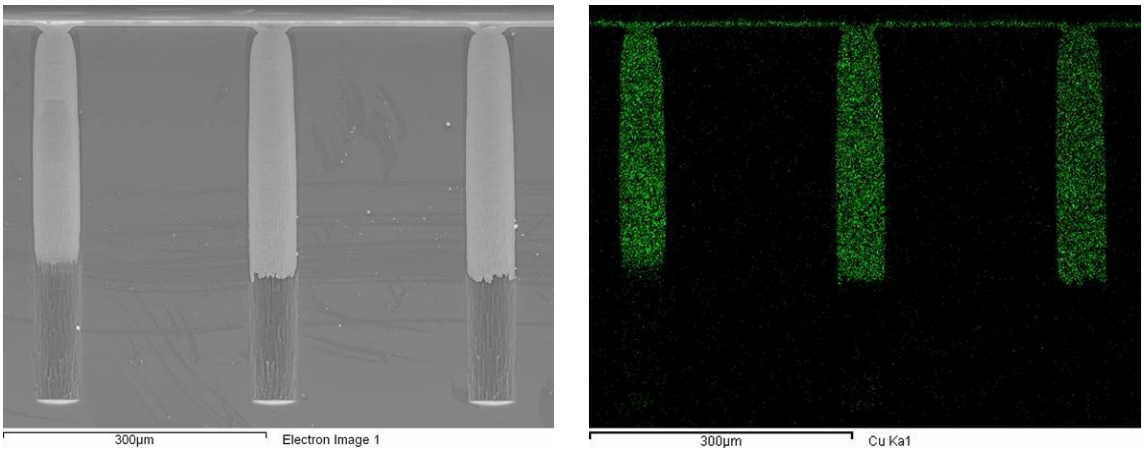


Figure 2.4: Cu element mapping using EDS. Left figure: SEM image of the cross-section of annular Cu vias; Right figure: Cu $K_{\alpha 1}$ X-ray mapping (green area).

The dimensions of annular vias are measured from the cross-section of the specimen using a SEM/FIB system (FEI Strata™ DB235). Table 2.1 lists the averaged height and thickness of the annular via structure.

Table 2.1: Bending beam sample dimension

Annular via array (D_f: 90 μm, p: 360 μm)	Unit: micron
Thickness of Wafer	710 ± 3
Height of via hole	429 ± 5
Height of Cu via	311 ± 7
Thickness of annular Cu via	1.6 ± 0.3
Thickness of silicon oxide	2.0 ± 0.2

To complete the TSV test structure, the overburden layers of silicon oxide and Cu on the wafer surface are mechanically polished off using 3-micron grade polycrystalline diamond suspension. The top Si surface is exposed after polishing. The finished bending beam specimen is illustrated in Figure 2.5a, and two oblique view SEM images are shown in Figure 2.5b and 2.5c, respectively.

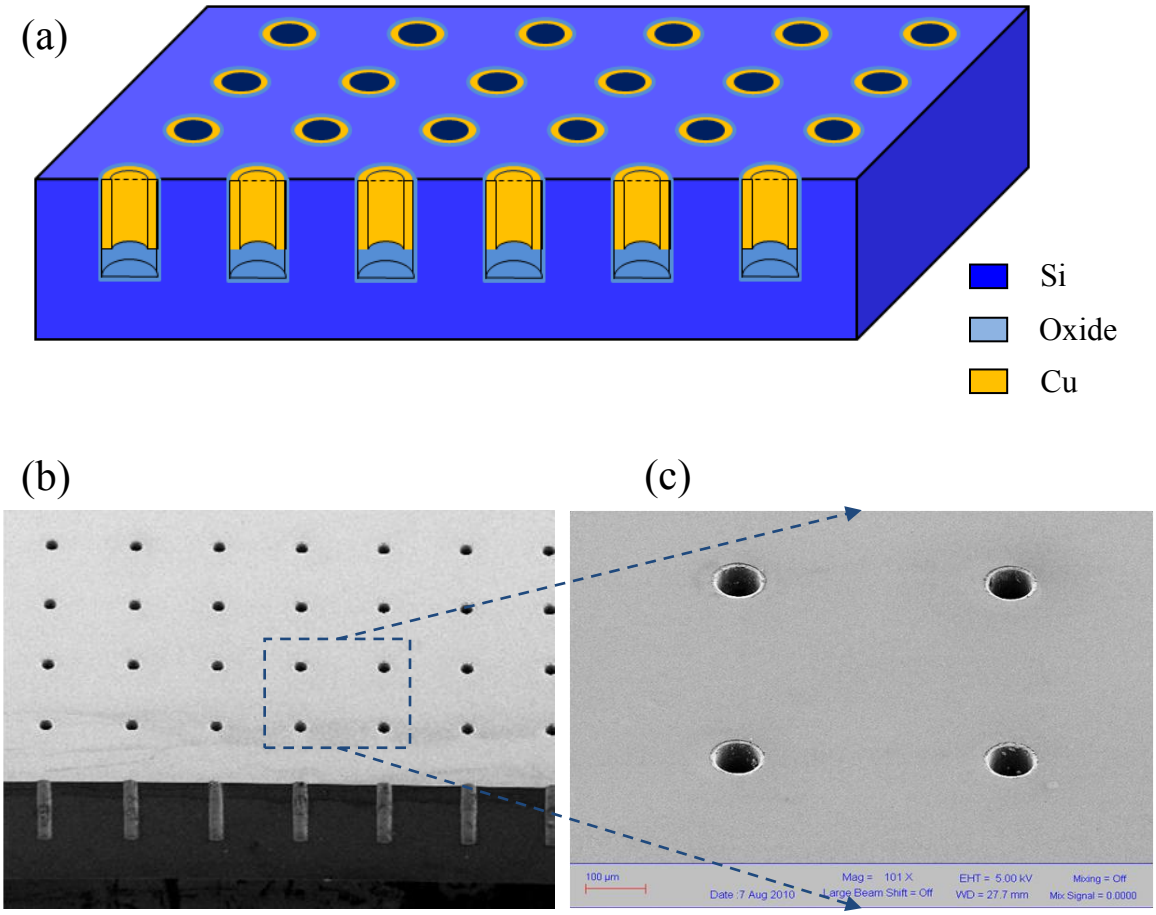


Figure 2.5: (a) Visual illustration of bending beam specimen; (b) & (c) Oblique view SEM images of a square grid annular Cu via array. Via diameter: 90 µm. Pitch: 450 µm.

2.2.3 Bending beam experiment and results

After the sample preparation, a specimen containing 90 μm Cu vias is selected for the bending beam experiment. The pitch size between adjacent vias is 360 μm. The specimen is placed in a vacuum test chamber with a 100 Torr of ambient dry nitrogen. The specimen is placed upside down on a supporting stage so that the incident laser beams are reflected by the backside of the specimen, i.e. the side without vias. If the front side (i.e. the side containing via array) is selected as the reflecting surface, incident laser beams will be diffracted by the periodic via array, yielding multiple diffracted laser spots on the photo sensors and false signals in the position indicator.

To start the stress measurement, the bending beam specimen is thermal-cycled between the room temperature and 200^{o}C in the vacuum chamber. The bending curvature of the specimen is continuously tracked as a function of the sample temperature. Several factors contribute to the bending of the specimen: (a) the thermal expansion of Cu vias, (b) the thermal expansion of silicon oxide liner, and (c) the initial curvature of the bare Si beam. To extract the contribution from the Cu vias to the beam bending, the baseline curvatures induced by (b) and (c) have to be subtracted off from the bending observed for the via test structure. For this reason, Cu vias are etched off from the test specimen using a nitric acid solution, and the baseline curvature is measured again under thermal cycles. By subtracting off the baseline curvature, the bending induced by the thermal expansion of the Cu via array is deduced.

Following this procedure, the bending curvature induced by Cu vias is obtained, and the result is plotted in Figure 2.6 as a function of temperature. The result shows clearly that the deformation of the Cu vias exhibits hysteresis loops during two thermal cycles between 30^{o}C and 200^{o}C. Since Si and silicon oxide are both linear elastic in nature, the hysteresis behavior observed can be attributed to plasticity of the Cu layer in

the via. This will be further discussed in the next section where the observed bending curvature in Figure 2.6 will be analyzed to deduce the stress characteristics of the via structure.

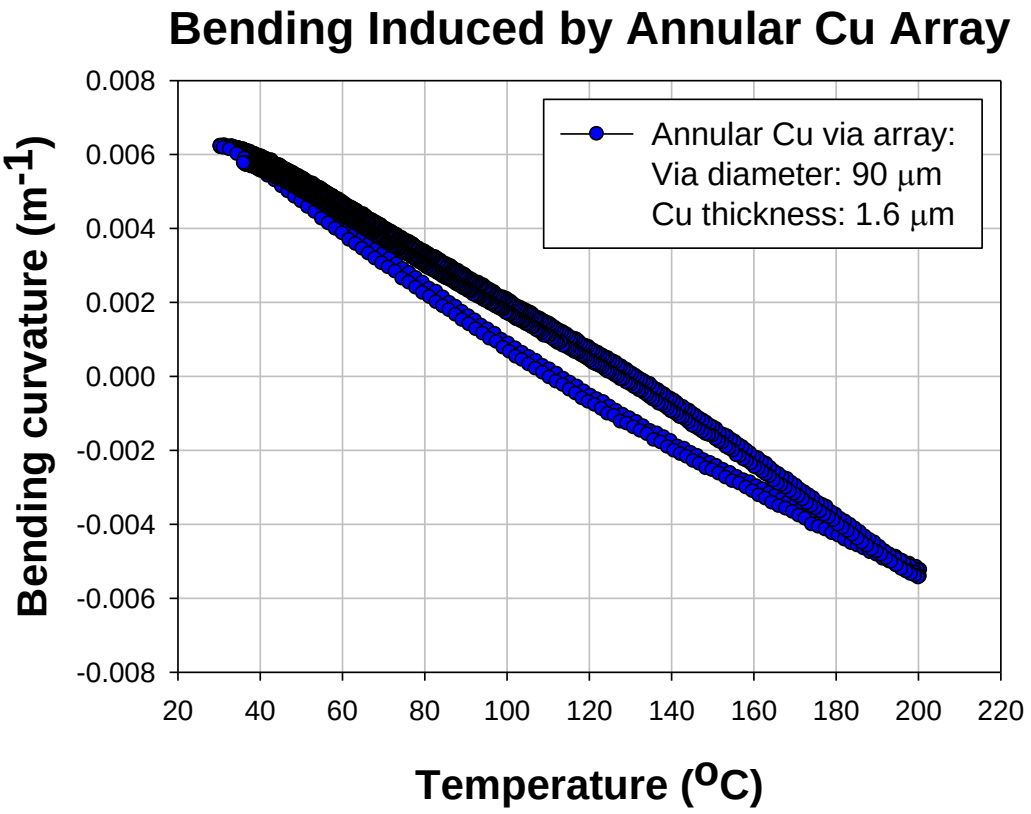


Figure 2.6: Bending curvature induced by periodic annular Cu array under repeated thermal cycles between 30°C to 200°C.

2.3 THERMAL STRESS ANALYSIS FOR ANNULAR CU VIAS

In this section, the thermal stress characteristics are deduced from the bending curvature of the Cu via structures observed during thermal cycling. In this analysis, an analogous example of stress measurement of a thin film is first described. Consider an

isotropic thin film lying on top of a thick Si substrate. Given a thermal loading, the thermal stress on the thin film is equal-biaxial and 2-D in nature where there is no out-of-plane stress. Assuming that the thin film thickness h_f is much thinner than the substrate thickness h_s, the equal-biaxial stress of the thin film, σ_f, is proportional to the curvature induced by the film, $\kappa - \kappa_o$:

$$\sigma_f = \frac{B_s h_s^2}{6h_f}(\kappa - \kappa_o), \qquad (2.2)$$

where B_s is the biaxial modulus of the substrate. Equation 2.2 is the well-known Stoney's equation [25].

Now consider the case of annular Cu vias embedded in the Si matrix as shown in Figure 2.5. Inside an annular Cu via, the thermal expansion mismatch between Cu and the Si matrix can induce thermal stresses during thermal cycling along the radial direction (σ_{rr}), the circumferential direction ($\sigma_{\theta\theta}$), and the axial direction (σ_{zz}). The stress state in such a Cu via is 3-D in nature, and the bending curvature of the whole Si beam is induced by the radial stress σ_{rr} and the circumferential stress $\sigma_{\theta\theta}$. Due to the different geometry, the stress components cannot be deduced simply from the bending curvature based on Equation 2.2. In this study, FEA is used to calculate the stress behavior of the Cu TSV test beam and to establish the relationship between the bending curvature and the stress components during thermal cycling. Based on the observed bending curvature, the stress components of the Cu via can be deduced. The FEA simulation procedure is described in the following section.

2.3.1 FEA simulation for annular Cu vias

The thermal stress-induced bending curvature is simulated using a finite element software (ANSYS®). A simplified FEA model containing a 5-by-2 square grid annular Cu via array is constructed, as illustrated in Figure 2.7a. In this FEA model, the height of annular Cu vias is less than half of the thickness of Si wafer (Figure 2.5a). The geometrical dimensions of annular Cu vias have been described in the previous section (see Table 2.1). A 3-D solid element (SOLID185) in the ANSYS® software is selected for simulation. The elemental mesh in one of the ten unit cells is shown in Figure 2.7b, while the elemental mesh of the annular Cu/silicon oxide is shown in Figure 2.7c. The thermo-mechanical properties of materials used for simulations are listed in Table 2.2. Among them, the CTE of silicon oxide is assumed to be the same as that of Si. By excluding the CTE mismatch between silicon oxide and the Si substrate, the bending curvature can be considered to be induced only by the mismatch of the thermal expansion between Si and the Cu vias.

A symmetric boundary condition is applied on the surfaces at x = 0 and at y = 0. The FEA model is simulated given a thermal load $\Delta T = -200^{o}C$. After the simulation is complete, the bending curvature and the stress components are extracted from the result files for discussion in the following sections.

Table 2.2: Thermo-mechanical properties of materials [26-28]

Material	CTE (ppm/K)	Young's Modulus (GPa)	Poisson's ratio
Si	2.3	130	0.28
Cu	17	110	0.35
Silicon oxide	2.3[1]	76	0.18

[1]The CTE of silicon oxide is assumed to be the same as that of Si.

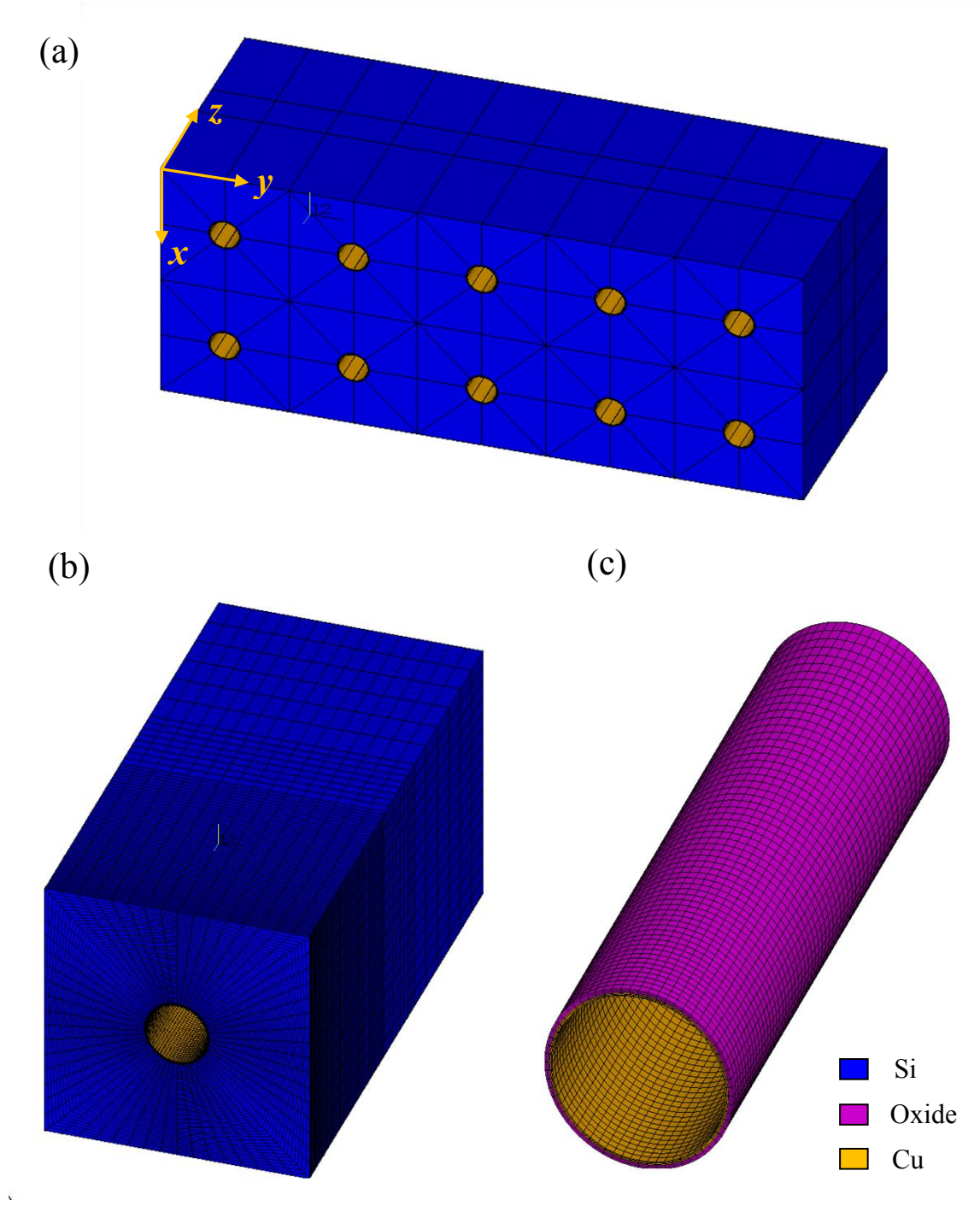


Figure 2.7: (a) FEA model containing a 5-by-2 annular Cu via array. (b) Element mesh in one via unit cell. (c) Element mesh in annular Cu via and the silicon oxide liner.

2.3.2 Thermal stresses on top Si surface

The FEA-simulated thermal stresses on the top Si surface are first analyzed. In a cylindrical coordinate system, the stress components are axi-symmetric. According to the semi-analytical near-surface solution [26], the radial stress σ_{rr} and the circumferential stress $\sigma_{\theta\theta}$ on the top Si surface (Figure 2.7a, z = 0) are of the same magnitude but opposite in sign. The out of plane stress component σ_{zz} vanishes on the surface. For simplicity, only the radial stress from FEA simulation is examined here. The distribution of σ_{rr} obtained by FEA is plotted as a function of the radial distance r in Figure 2.8. Under an increasing thermal load ΔT, the bending curvature of the FEA model increases linearly with the thermal load. The radial stress distribution also increases uniformly with the bending curvature on the top Si surface.

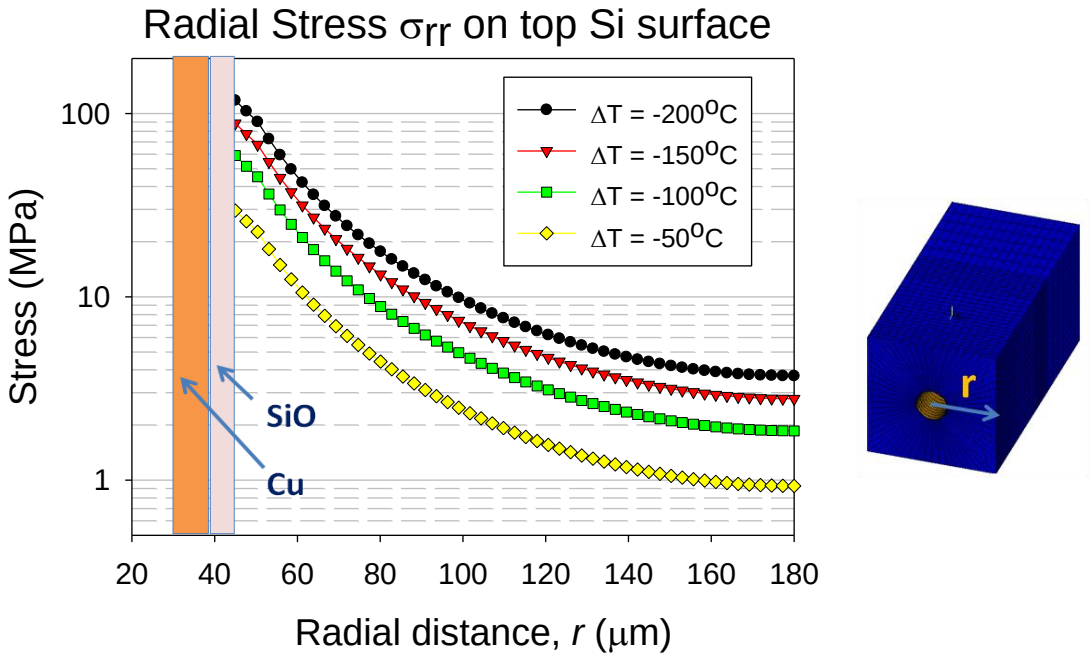


Figure 2.8: Distribution of radial stress σ_{rr} on the top Si surface under an increasing thermal loading.

Further examination of Figure 2.8 reveals that the radial stress is proportional to the bending curvature. As an example, the simulation result for a radial coordinate $r = D_f/2$ (with the $r = 0$ at via center) on the top Si surface (z = 0) is selected for discussion. Figure 2.9 plots the radial stress versus the bending curvature, where the FEA result exhibits a linear relationship between the radial stress and the bending curvature. The linear equation shown in Figure 2.9 can be used to deduce the radial stress once the bending curvature of the test beam is determined.

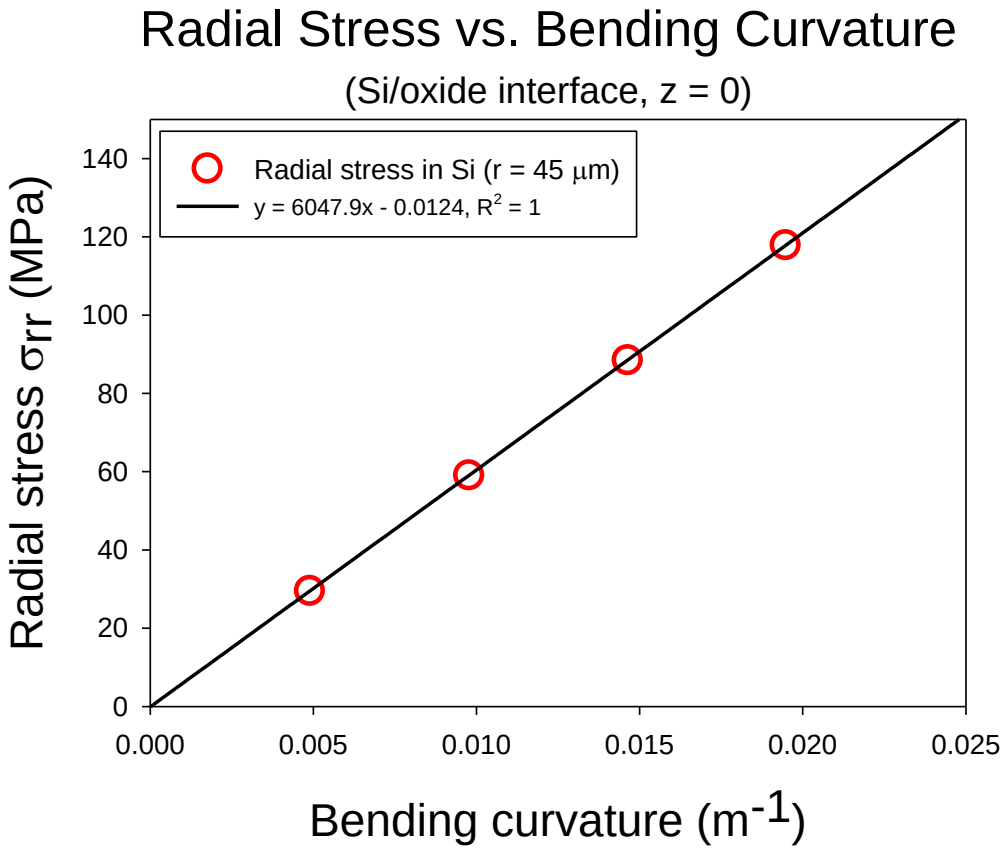


Figure 2.9: A linear relationship between the bending curvature and the radial stress σ_{rr} at a specific location (top Si surface, Si/silicon oxide interface).

After establishing the stress-curvature relationship using FEA, the bending curvature from the bending beam experiment is converted to the radial stress for the selected location ($r = D_f/2$, z = 0). This corresponds to the circumference of the Cu TSV on the top Si surface where the radial stress can be deduced from the measured beam curvature and the result is plotted in Figure 2.10 as a function of temperature for the two thermal cycles. The results show that the bending beam specimen has a stress-free temperature of 112°C or 125°C, depending on whether a positive or negative thermal load is applied. The non-linear stress-temperature curve results from the plasticity of Cu material during thermal cycles, which is discussed in the next section.

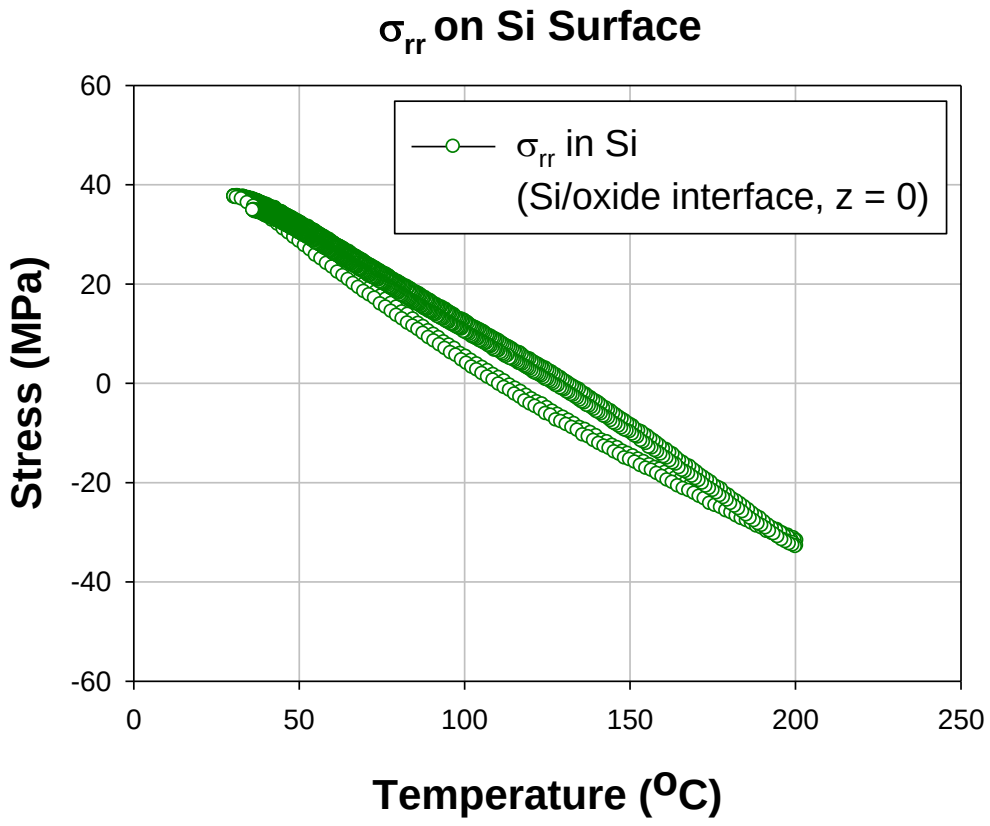


Figure 2.10: Radial stress σ_{rr} vs. temperature (top Si surface, Si/silicon oxide interface).

2.3.3 Thermal stresses in annular Cu vias

Here the FEA-simulated thermal stresses in an annular Cu via are analyzed. In a cylindrical coordinate system, the thermal stress distribution in the annular Cu via is also axi-symmetric. Under a thermal load $\Delta T = -100^{o}C$, thermal stresses in Cu along the Cu/oxide interface are plotted as a function of depth z in Figure 2.11.

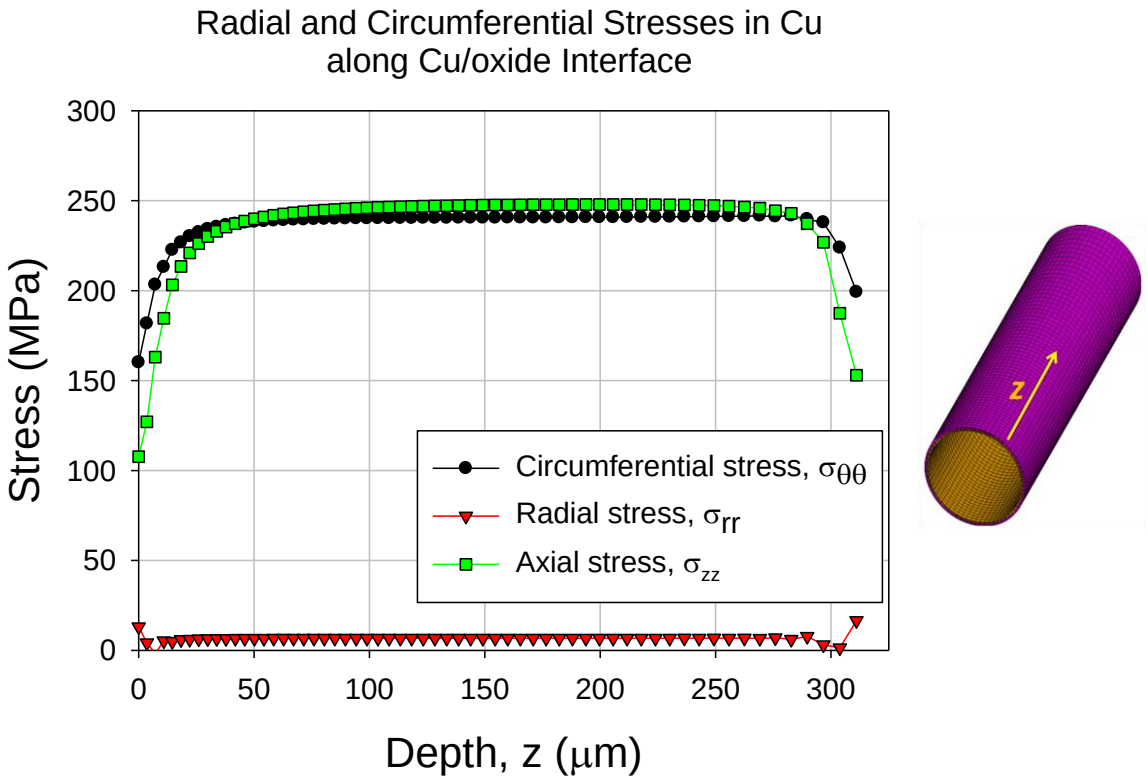


Figure 2.11: Stresses in annular Cu as a function of depth z (Cu/oxide interface).

As shown in Figure 2.11, the circumferential stress $\sigma_{\theta\theta}$ and the axial stress σ_{zz} are of a similar magnitude, but the radial stress σ_{rr} is smaller than circumferential stress by a factor of 20. This can be attributed to the fact that the thickness of annular Cu is

much thinner than the via diameter D_f so that the stress state is equivalent to that of a thin Cu film under thermal loading. It is interesting to note the stress variation as a function of the depth where the stresses approach a steady-state at a distance ~D_f away from both ends of the Cu cylinder. Therefore, over most of the annular Cu via, except near the ends, the stress state may be approximated by a 2-D plane-strain solution for a thin-wall cylinder.

In the following, the stress components which contribute to beam bending (σ_{rr} and $\sigma_{\theta\theta}$) are chosen for analysis. As an example, FEA results at a depth z = D_f on the via/ oxide interface are selected for discussion. FEA-simulated thermal stresses in Cu are plotted as a function of the bending curvature in Figure 2.12. Linear equations between stresses and the bending curvature are obtained by curve fitting.

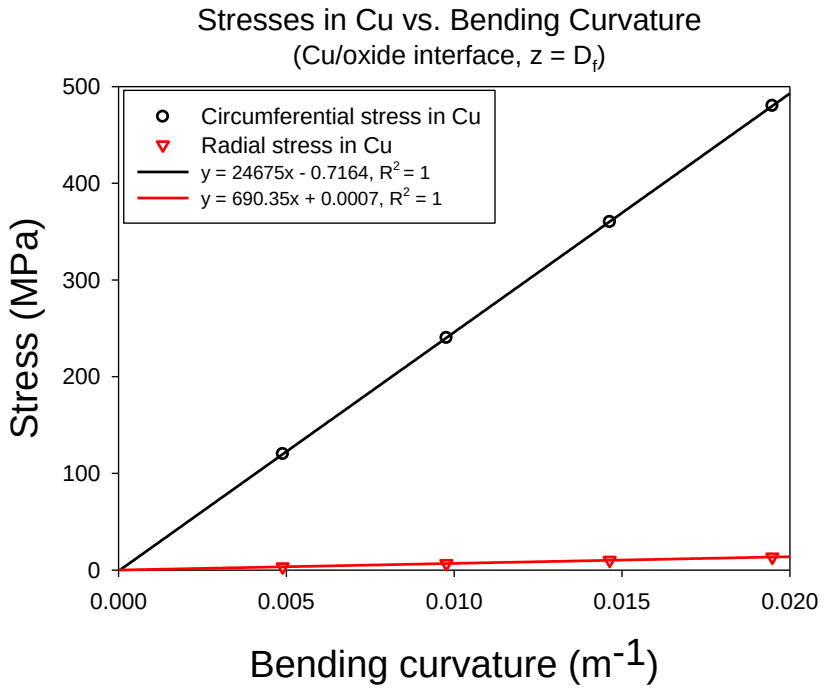


Figure 2.12: Linear relationship between the bending curvature and the σ_{rr} and $\sigma_{\theta\theta}$ in annular Cu via (Cu/silicon oxide interface).

The stresses in annular Cu vias at z = D_f can be deduced based on the linear relations established by FEA simulations (Figure 2.12) and the bending curvature observed (Figure 2.6). It should be pointed out that such linear relationships between the stresses and the bending curvature applies no matter whether the Cu material has been yielded or not. The bending curvature of the Si beam originates from the force balance between the Si beam and the via structures on top. Because the Si material is linear elastic, the force (or stress) required to bend the Si beam is linearly proportional to the bending curvature.

The radial and circumferential stresses at the chosen location ($r = D_f/2 - t_{oxide}$, z = D_f) are plotted as a function of temperature in Figure 2.13.

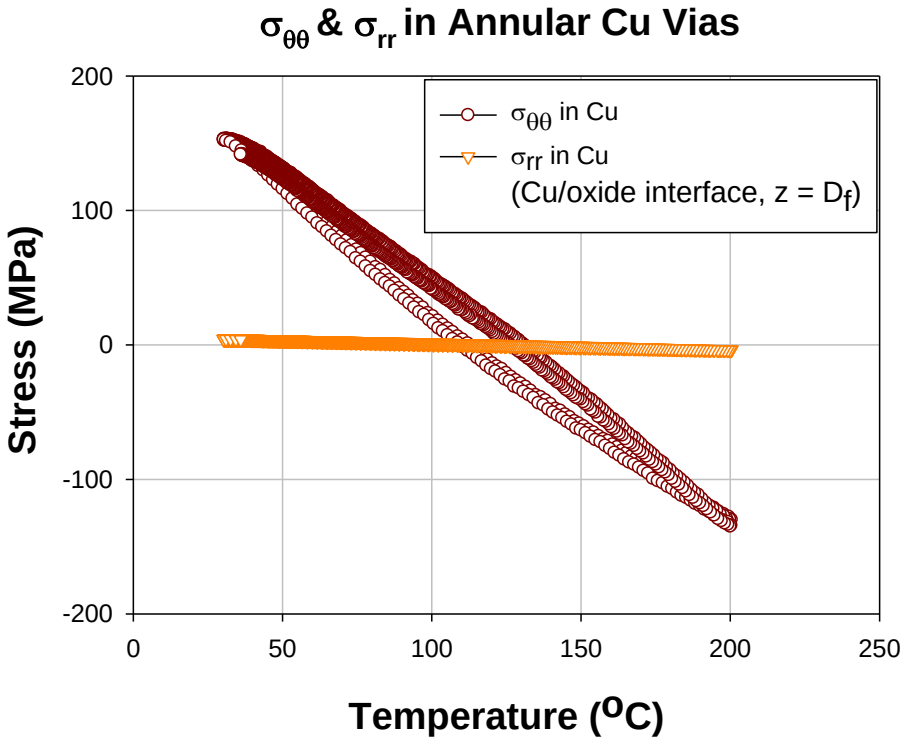


Figure 2.13: Stress-temperature curves of annular Cu vias (Cu/silicon oxide interface).

In Figure 2.13, the radial stress in the annular Cu via is almost zero. It is expected because of the traction-free surface on the inner side wall of the via. The circumferential stress, which is much large than the radial stress, ranges from +150 MPa (at 30^{o}C) to -130 Mpa (at 200^{o}C). It impies that only the circumferential stress (or force) in Cu vias acocunts for the specimen bending, becuse the other stress components σ_{zz} and σ_{rr} have a minimum contribution to the bending. The other observation from Figure 2.13 is the elastic hysresis behavior of Cu. The annular Cu via is subjected to a thermal load followed by another reverse thermal load. During the reverse loading, the annualr Cu via exhibits an initial elastic unloading curve, followed by a so called "early yielding" behavior occuring at a stress level below 50 MPa. Early yielding is often observed in thermal stress measurements for metallic thin films, which is similar to the Bauschinger effect in bulk metals. Dislocation theories were applied in the past to explain such early yielding behavior of Cu thin films [29]. Because the annular Cu via investigated here is only ~1.6 μm thick, the annular Cu via is equivalent to a Cu thin film. The observed "early yielding" behavior may be the same as that of Cu thin films.

2.4 SUMMARY

A stress measurement on Cu via arrays using bending beam technique has been demonstrated in this Chapter. The state-of-the-art curvature measurement technique has a sensitive resolution of 10^{-3} m^{-1} in curvature, making it possible to detect the beam deflection induced by a small magnitude of stress in Si (< 50 MPa). It has been found challenging to measure the stresses in such annular via structure using other techniques such as micro-Raman.

Bending beam technique can also be used to observe the plasticity behavior of Cu material during thermal cycling. In Figure 2.13, a non-linear elastic behavior has been observed in the electroplated Cu material, and the stress-free temperature of Cu vias can be determined from such stress-temperature curve. Comparing to micro-Raman measurements, which are often operated at room temperature, the bending beam technique provides useful temperature-dependent information for thermo-mechanical analyses. However, the major disadvantage of the bending beam method is the sample preparation, which requires a large population of periodically arranged vias. The other disadvantage of this technique is that only averaged global stresses/strains of the whole beam are measured. Such a technique cannot measure individual vias as micro-Raman does. The local stresses in individual vias are subjected to the variation in Cu thickness, the variation in oxide thickness, the elastic anisotropy in Cu grains, etc. The precise local stresses induced by a specific TSV cannot be obtained using FEA simulations with averaged sample geometry and with isotropic material properties. Instead, TSV-induced local stresses near the Si surface can be measured using micro-Raman. Consequently, for one to characterize the thermal stresses in TSV structures, the bending beam method and micro-Raman can be employed together as complementary techniques.

Chapter 3: Through-Silicon-Via (TSV)-Induced Thermal Stresses in Silicon Substrates and Piezoresistivity Effect on MOSFETs

3.1 INTRODUCTION

With continuing device scaling, traditional wiring design imposes significant challenges on the device performance, power dissipation, and packaging form factor. This has generated great interest recently in developing 3-D integration [30], [31],[31],[32]. While the current effort has been focused on design and processing developments, the reliability challenges due to 3-D integration cannot be overlooked. Specifically, the incorporation of through-silicon-via (TSV) structures can significantly impact the thermo-mechanical reliability of 3-D interconnects. The mismatch in thermal expansion between the TSV and Si can induce large thermal stresses during TSV fabrication to degrade the performance of stress-sensitive devices. It has been reported that 100 MPa of stress can change by over 7% the carrier mobility in MOSFET devices [33]. Thus the stress impact on device performance has to be considered in 3-D integrated circuits. Stress analyses using numerical and analytical methods have been conducted in the past to address these reliability issues. The TSV-induced piezoresistivity effect on MOSFETs has also been investigated [19]. Nevertheless, further studies are required to understand the impact of material properties and TSV geometry on the overall stress behavior and the design of the keep-out zone (KOZ) for MOSFET devices.

In this chapter, TSV-induced thermal stresses in Si are first analyzed. FEA simulations and analytical solutions are used to characterize the stress distribution in the Si wafer surrounding an isolated TSV. Here the analysis is focused on the near surface region in the Si surrounding the TSV since most of the devices are fabricated very close (about 1 μm) to the surface. This is followed by examining the piezoelectric effect induced by the near surface stresses on the charge mobility for p- and n- channel

MOSFET devices. This provides the basis for the design of the KOZ for MOSFET devices. Finally, the possibility for optimization of the KOZ design is explored by performing parametric studies investigating the effect of TSV scaling, dielectric liner, and material and geometry of TSVs .

3.2 TSV-INDUCED THERMAL STRESS NEAR THE SI WAFER SURFACE

In this section, the distribution of TSV-induced thermal stress in Si is investigated. A semi-analytical, near-surface stress solution is first reviewed in Section 3.2.1, and then is compared with FEA simulations in Section 3.2.2. The semi-analytical solution has a good agreement with FEA simulations, and they together reveal the characteristics of TSV-induced thermal stresses in a cylindrical coordinate system. In Section 3.2.3, TSV-induced thermal stresses in the Cartesian coordinate system is investigated for better understanding of the stress components which impact the device performance. In Section 3.2.4, the effect of elastic anisotropy of Si is investigated using FEA simulations in the Cartesian coordinate system.

3.2.1 Semi-analytical stress solutions

The stress field induced by differential thermal expansion in the via and Si is three-dimensional in nature. For simplicity, here a 2-D stress solution is first introduced [26]. Consider an infinitely long TSV embedded in an infinitely thick Si wafer under a thermal load ΔT. In a cylindrical coordinate system, the stress field in the Si matrix is axi-symmertric, varying with the radial distance *r* measured from the center of TSV. The thermal stress in Si can be expressed using a 2-D plane-strain solution:

$$\sigma_r^{Si} = -\sigma_\theta^{Si} = \frac{-E_f \varepsilon_T}{1-2\nu_f + \frac{1+\nu_m}{1+\nu_f}\frac{E_f}{E_m}}\left(\frac{D_f}{2r}\right)^2$$

$$\sigma^{Si}{}_{r\theta} = \sigma^{Si}{}_{rz} = \sigma^{Si}{}_{\theta z} = \sigma^{Si}{}_{z} = 0 \quad , \tag{3.1}$$

where σ_r and σ_θ are the radial and circumferential stresses, respectively, $\varepsilon_T = (\alpha_f - \alpha_m)\Delta T$ is the mismatch strain due to a thermal load ΔT. D_f is the diameter of the TSV. The material properties, α, E, ν, are the coefficient of thermal expansion (CTE), Young's modulus, and Poisson's ratio, with the subscripts f and m for the via (fiber) and Si (matrix), respectively. For a Cu TSV, the Young's modulus of electroplated Cu is 115 GPa [34], which is close to that of a (001) Si wafer (130 ~ 169 GPa, [27]). Therefore, by neglecting the elastic mismatch between Cu and Si, Equation 3.1 can be simplified to:

$$\sigma_r^{Si} = -\sigma_\theta^{Si} = \frac{-E\ \varepsilon_T}{2(1-\nu)}\left(\frac{D_f}{2r}\right)^2 , \tag{3.2}$$

where $E = E_f = E_m$ and $\nu = \nu_f = \nu_m$ are assumed. Equation 3.1 and Equation 3.2 depict an axi-symmetric stress distribution surrounding the TSV. The magnitude of stresses in Si decays with the square of the ratio between the radial distance r and TSV diameter D_f. The maxima of σ_r and σ_θ occur at the boundary of the TSV ($r = D_f/2$),

and are independent of the TSV diameter D_f. Instead, the maximum stresses are mainly controlled by the thermal expansion mismatch $\alpha_f - \alpha_m$ and thermal load ΔT.

The above 2-D solutions are valid under a plane-strain condition for an infinitely long TSV. To deduce the thermal stresses near the wafer surface, a 3-D semi-analytical solution has been developed using a superposition method by Ryu et al [26]. Such 3-D semi-analytical solution is briefly reviewed in the following. Under the assumption of linear elasticity, the stress field near the wafer surface can be obtained by superposition of the solutions for two problems. Such two problems are illustrated in Figure 3.1.

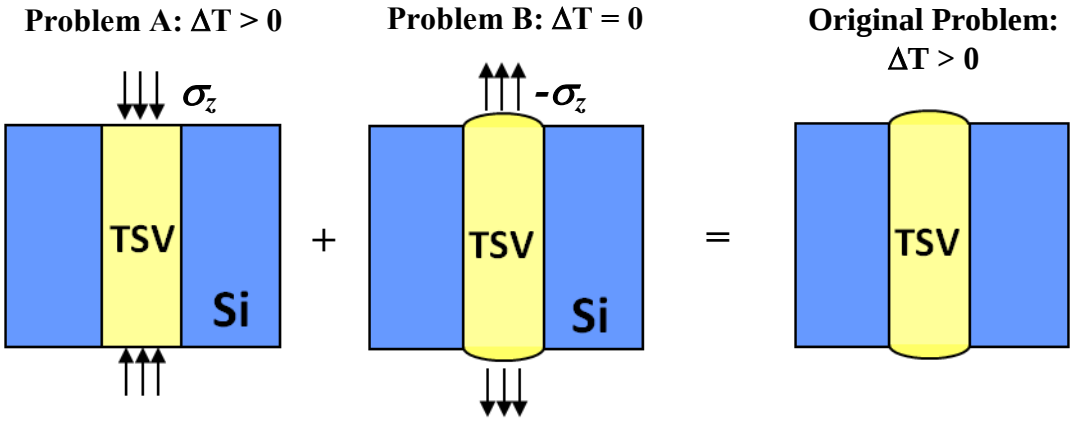


Figure 3.1: Illustration of the superposition of two problems: (a) Problem A, a surface traction with a thermal load ΔT; (b) Problem B, an opposite surface traction without thermal load; (c) the original problem. (Courtesy of Ryu, Suk-Kyu in Ref. [26])

For problem A, the system is subjected to a thermal load (ΔT) and a fictitious stress (σ_z) on the surfaces of the via, so that the stress field in such a TSV structure is

homogeneous along the axial/depth direction. Problem A is equivalent to the aforementioned 2-D plane-strain problem, and the stress field in Si can be expressed as Equation 3.1. To recover the traction-free boundary condition on the surfaces in the original problem, the fictitious stress is removed by superimposing problem B, in which the TSV is subjected to an opposite pressure of the same magnitude ($p = \sigma_z$) at both ends, but no thermal load. For problem B, an approximate solution can be obtained semi-analytically (Ryu, et al. in Ref. [26]). By ignoring the elastic mismatch between TSV and Si, the semi-analytic solutions for σ_r and σ_θ in problem B are expressed as follows:

$$\sigma_r^B(r,z) = \frac{-E\varepsilon_T}{2\pi(1-\nu)} \int_0^{\frac{D_f}{2}} \int_0^{2\pi} \left[\left(\frac{1-2\nu}{R^2+Rz} - \frac{3z(R^2-z^2)}{R^5} \right) \cos^2\beta + \left(\frac{z}{R^3} - \frac{1}{R^2+Rz} \right)(1-2\nu)\sin^2\beta \right] \rho \, d\rho \, d\theta \quad , \tag{3.3}$$

$$\sigma_\theta^B(r,z) = \frac{-E\varepsilon_T}{2\pi(1-\nu)} \int_0^{\frac{D_f}{2}} \int_0^{2\pi} \left[\left(\frac{1-2\nu}{R^2+zR} - \frac{3z(R^2-z^2)}{R^5} \right) \sin^2\beta + \left(\frac{z}{R^3} - \frac{1}{R^2+zR} \right)(1-2\nu)\cos^2\beta \right] \rho \, d\rho \, d\theta \quad , \tag{3.4}$$

where $R = \sqrt{z^2 + \rho^2 + r^2 - 2\rho r\cos\theta}$ and $\beta = \tan^{-1}\left(\frac{\rho\sin\theta}{r - \rho\cos\theta} \right)$. In a cylindrical coordinate system, σ_r^B and σ_θ^B are axi-symmertric, varying with the radial distance *r* and the depth z with z = 0 at the top Si surface. Unlike problem A, where the

radial stress σ_r and the circumferential stress σ_θ are of the same magnitude but opposite in sign (Equation 3.1, 3.2), the magnitude of σ_r^B and σ_θ^B in problem B are not necessary the same (Equation 3.3, 3.4).

The stress field in the original problem is the summation from problem A and B. Since the thermal stresses of interest to the later calculation of the piezoresistivity effect are very near the Si surface, σ_r and σ_θ on the surface are examined. By combining Equation 3.2, 3,3, and 3.4, The radial stress σ_r and the circumferential stress σ_θ on the Si surface (i.e. z = 0) can be expressed in Equation 3.5:

$$\sigma_r = -\sigma_\theta = \frac{-E\ \varepsilon_T}{2(1-\nu)}\left(\frac{D_f}{2r}\right)^2 + \frac{-E\varepsilon_T}{2\pi(1-\nu)}\int_0^{\frac{D_f}{2}}\int_0^{2\pi}\frac{(1-2\nu)\cos 2\beta}{\rho^2 + r^2 - 2\rho r\cos\theta}\rho\, d\rho\, d\theta\,, \quad (3.5)$$

Here σ_r and σ_θ in Equation 3.5 remain axi-symmetric, varying with the radial distance r. Note that such two stress components on the Si surface are of the same magnitude but opposite in sign. In the next section, thermal stresses deduced from the semi-analytical solution will be compared with the results from FEA simulations for a specific TSV geometry.

3.2.2 Comparison between analytical solutions and FEA simulation

Here a FEA simulation is performed to compare with the 3-D semi-analytical solutions (Ryu, et al. [26]). In the following, TSV-induced radial stress σ_r is first simulated using FEA and then is compared to the summation of Equation 3.2 and 3.3. An axi-symmetric FEA model is constructed using the ANSYS® software, as illustrated in Figure 3.2. The TSV diameter D_f is 20 μm and the wafer thickness H is 200 μm. A 2-D plane element (PLANE182) in the ANSYS® software is selected for simulation. The reference temperature of both Cu and Si are assumed to be the same, and then a negative thermal loading, ΔT = -250°C, is applied. The material properties used in the FEA are: $E_f = E_m = 110$ GPa, $\nu_f = \nu_m = 0.35$, and $\alpha_f = 17$ ppm/℃ and $\alpha_m = 2.3$ ppm/ ℃. The model is an approximation to a Cu TSV embedded in Si, ignoring the elastic mismatch between Cu and Si.

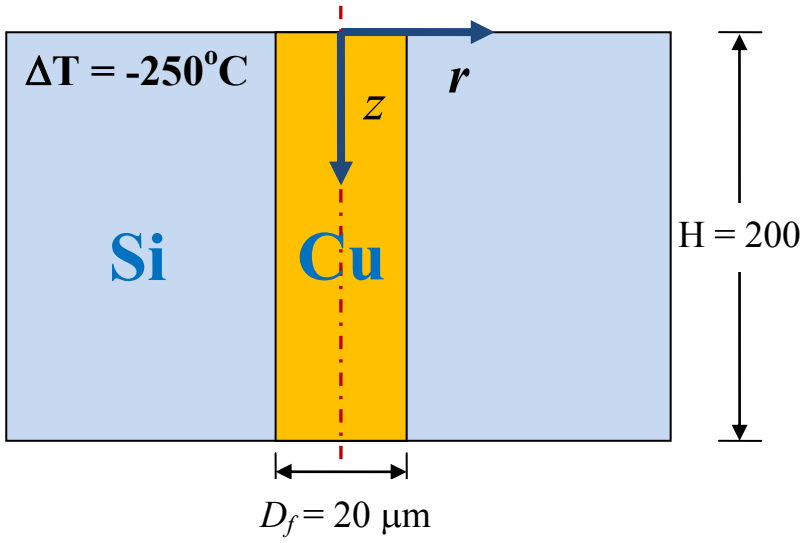


Figure 3.2: Illustration of the cross-section of an axi-symmetric FEA model for thermal stresses simulation.

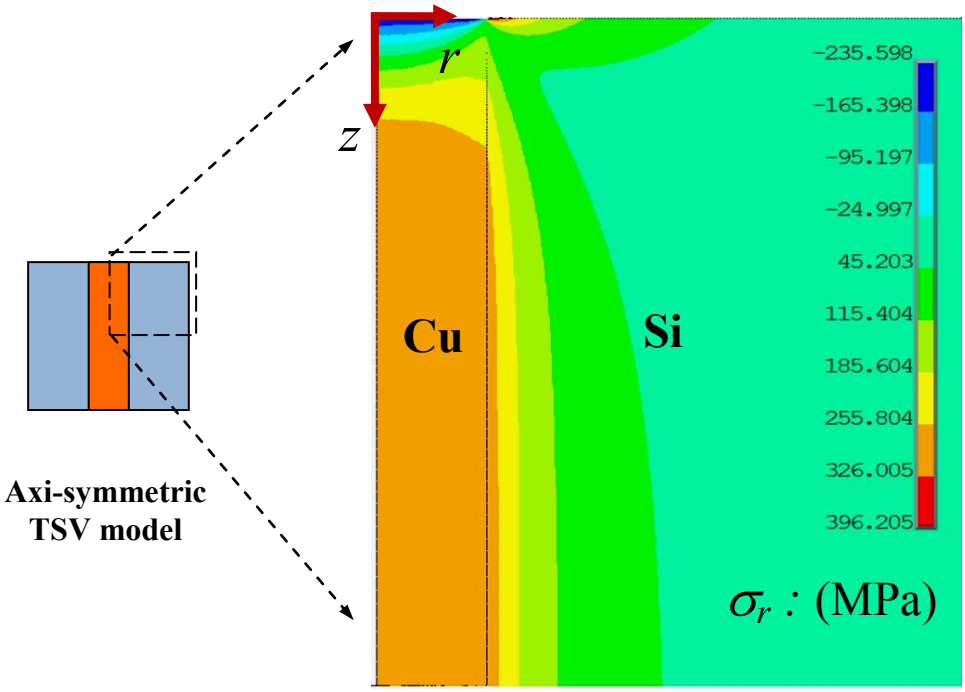


Figure 3.3: FEA simulation of the thermal stress component σ_r on the cross-section of TSV (D_f= 20 μm, ΔT = −250 ºC).

Figure 3.3 shows the distribution of the radial stress σ_r on the cross-section of the TSV model. In a cylindrical coordinate system, the radial stress σ_r is axi-symmetrically distributed, generally decreasing as a function of the radius r away from the center of the TSV. Given the negative thermal load, the shrinkage of Cu TSV near the wafer surface induces a maximum tensile radial stress in Si along the circumference of TSV. The magnitude of radial stress is depth-dependent near the wafer surface, and is stabilized at a depth z > $2D_f$.

To verify the semi-analytic solutions, Equation 3.2 and 3.3 are used to calculate the radial stress given the same TSV geometry and thermal load (D_f= 20 μm, ΔT = −250 ºC), and then the results are compared to those obtained from the FEA simulation in

Figure 3.4. In the figure, the radial stresses in Si are plotted as a function of the radial coordinate r measured from the center of TSV. The results are compared for three different depth (z = 0, D_f /2, and 5D_f), and there is a good agreement between the semi-analytic solution and the FEA simulation. According to the semi-analytic solution, the maximum radial stress on the wafer surface (z = 0) occurs at a short distance away from the edge of TSV, a characteristic which is also observed in the FEA simulation. In contrast, at a depth $z = D_f/2$, the maximum radial stress occurs right at the edge of TSV. When the depth z is deeper than $5D_f$ away from the top surface, the stress state approaches the plane-strain condition. In that case, the radial stress distribution obtained using FEA is similar to that calculated using the 2-D plane-strain solution (i.e. Equation 3.2 alone).

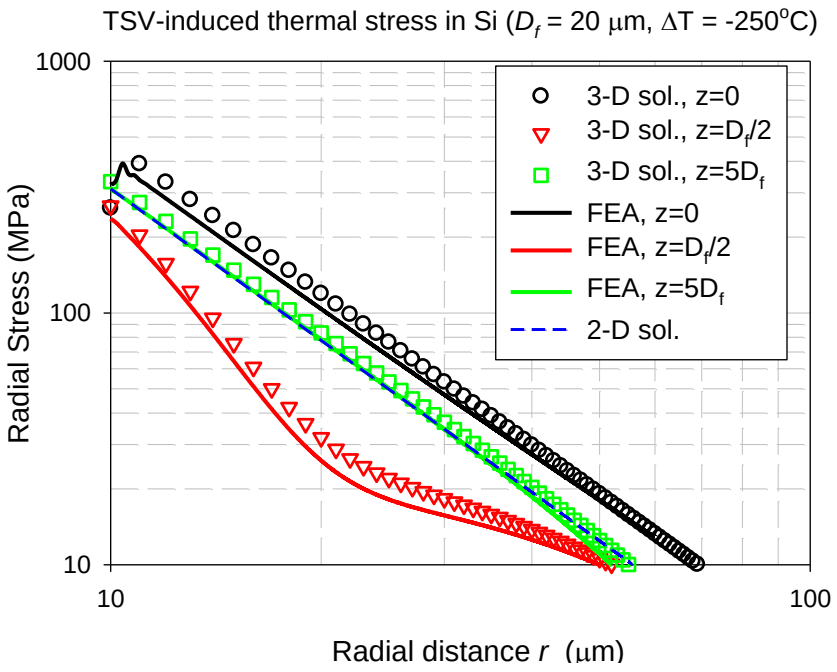


Figure 3.4: Comparison between semi-analytic stress solution and FEA simulation (in log-log scale).

3.2.3 Thermal stress distribution in Cartesian coordinate system

Virtually all the microelectronic devices on the Si wafer are manufactured in rectangular configurations, where the channel direction of MOSFETs is usually aligned along the <110> directions on a (001) Si wafer surface. To analyze the stress effects on the device characteristics, it is convenient to express the thermal stress distribution on the wafer surface in the Cartesian coordinate system. For simplicity, the stress characteristics are first discussed using the 2-D plane-strain solution (Equation 3.2). By transforming the coordinate from a cylindrical system to a Cartesian system, Equation 3.2 can be rewritten as:

$$\sigma_{xx} = -\sigma_{yy} = -\frac{E\varepsilon_T {D_f}^2 (x^2 - y^2)}{8(1-\nu)(x^2+y^2)^2}$$
$$\sigma_{xy} = -\frac{E\varepsilon_T {D_f}^2 xy}{4(1-\nu)(x^2+y^2)^2} \quad , \qquad (3.6)$$

where the TSV is located at the origin. From Equation 3.6, the normal stress σ_{xx} and shear stress σ_{xy} are obtained for a 20 μm TSV with an arbitrary thermal load. Figure 3.5 plots the spatial distribution of σ_{xx} and σ_{xy} on the TSV wafer surface in a Cartesian coordinate system. Here the stress distribution is not axi-symmetric, but has a two-fold rotational symmetry. It is seen that tensile and compressive stresses are concentrated along mutually perpendicular directions around the TSV. Due to the fact that the mobility change in MOSFETs is mainly controlled by the normal stresses, σ_{xx} and σ_{yy} , and is not sensitive to the shear stress σ_{xy} (see discussion in Section 3.3), the results here

indicate that the distribution of the mobility change is also two-fold rotationally symmetric.

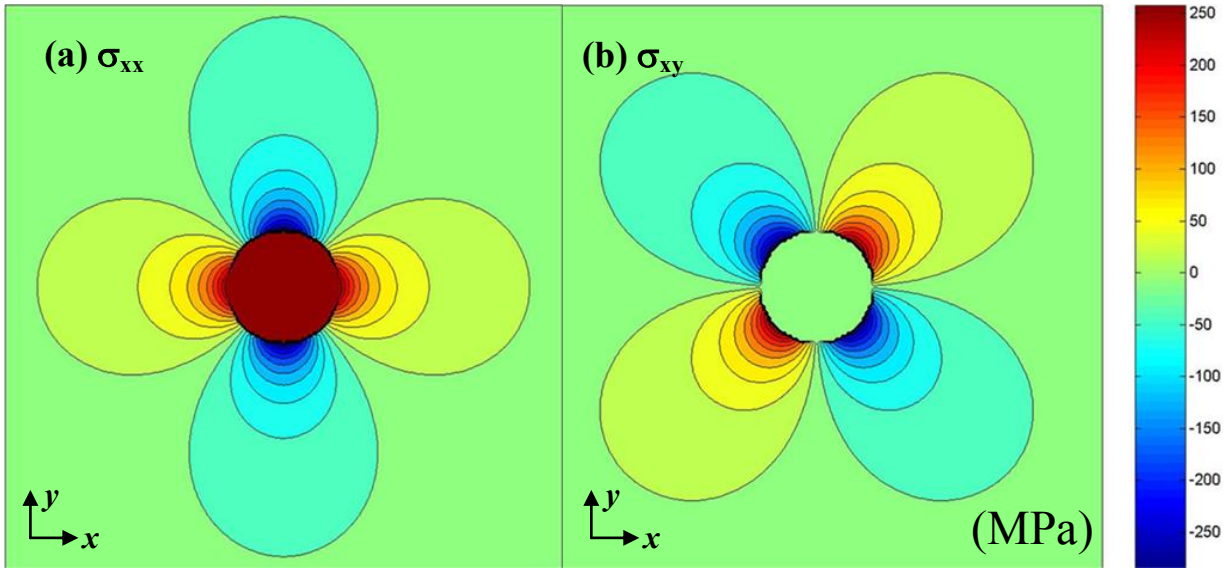


Figure 3.5: Thermal stress distribution in Cartesian coordinate system (D_f= 20 μm, ΔT = −175 ºC).

3.2.4 Effect of elastic anisotropy of silicon on thermal stress distribution (Cartesian system)

In the previous stress analyses, the TSV and Si materials are assumed to be elastically isotropic. In a real TSV structure, the Si substrate and metallic materials such as Cu and Ni are all anisotropic. Due to the anisotropic material properties, the thermal stress distribution in the Si substrate can be different from that in the previous analyses. In addition, TSVs often consist of polycrystalline metallic materials (see Figure 3.6).

During thermal cycling, the elastic anisotropy can yield a component of hydrostatic tensile stress near the grain boundary between crystal grains of different orientation. Such tensile stress can induce voiding in the polycrystalline Cu lines or Cu vias at an elevated temperature [35].

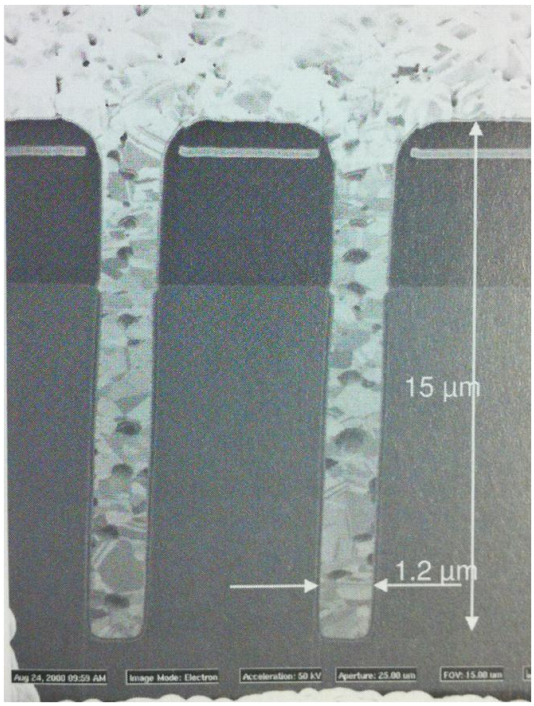


Figure 3.6: TSVs filled with polycrystalline CVD Cu (Source: Klumpp in Ref. [12]).

The effect of elastic anisotropy on the thermal stress distribution in Si is investigated here. In the following discussion, the Si substrate is assumed to be the most commonly used single crystalline (001) wafer. Because the TSV diameter (20 µm) is much larger than the grain size of Cu (Figure 3.6), the polycrystalline grain structure can reduce the effect of Cu anisotropy. Consequently, the Cu TSV is assumed to be elastically isotropic for simplicity.

The distribution of thermal stresses on the (001) Si wafer surface is simulated using FEA. A 3-D FEA model is constructed in ANSYS® software, as illustrated in Figure 3.7a. A 3-D solid element (SOLID185) in the ANSYS® software is selected for simulation, and the element meshes in a quarter of the model are shown in Figure 3.7b. The TSV diameter D_f is 20 μm and the wafer thickness H is 200 μm. In order to capture the stress distribution on the wafer surface, the element thickness on the top surface is reduced to 0.25 μm.

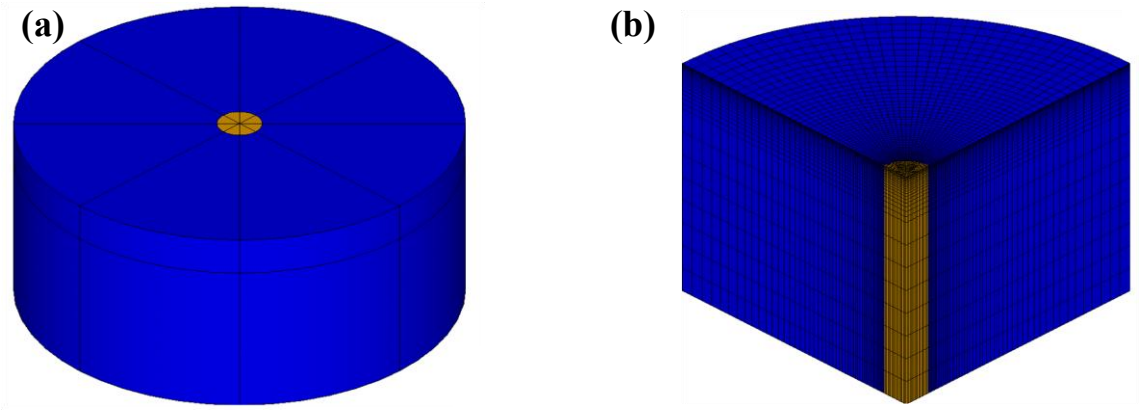


Figure 3.7: (a) FEA model of an isolated Cu TSV; (b) Element mesh in a quarter of the FEA model.

Table 3.1: Thermo-mechanical properties of the materials for FEA simulations [26-28], [36-39]

Material	CTE (ppm/K)	Young's Modulus (GPa)	Poisson's ratio
Si	2.3	130	0.28
Cu	17	110	0.35
Al	20	70	0.35
Ni	13	207	0.31
W	4.4	400	0.28
BCB	40	3.0	0.34
Silicon oxide	0.51	72	0.16

The isotropic material properties for Cu are taken from Table 3.1. To simulate the elastic anisotropy of Si, the following stiffness matrix for a (001) Si wafer is used as the material input in the ANSYS® software [27]:

$$C^{Si}_{(001)} = \begin{bmatrix} 166.2 & 64.4 & 64.4 & 0 & 0 & 0 \\ 64.4 & 166.2 & 64.4 & 0 & 0 & 0 \\ 64.4 & 64.4 & 166.2 & 0 & 0 & 0 \\ 0 & 0 & 0 & 79.8 & 0 & 0 \\ 0 & 0 & 0 & 0 & 79.8 & 0 \\ 0 & 0 & 0 & 0 & 0 & 79.8 \end{bmatrix} GPa$$

After constructing the FEA model with anisotropic Si, a negative thermal load $\Delta T = -200^{o}C$ is applied for simulation. The thermal stresses on the (001) Si wafer surface are extracted from the simulation results, and the distribution of normal stress σ_{xx} are plotted in Figure 3.8a and 3.8b with the x axis aligned with the [100] and [110] crystal direction, respectively. In the last, the simulation is performed on the same model except with isotropic Si properties (Table 3.1), and the distribution of σ_{xx} on such isotropic Si wafer surface is shown in Figure 3.8c. For the sake of comparison, the stress scales in Figure 3.8a, 3.8b, and 3.8c are normalized.

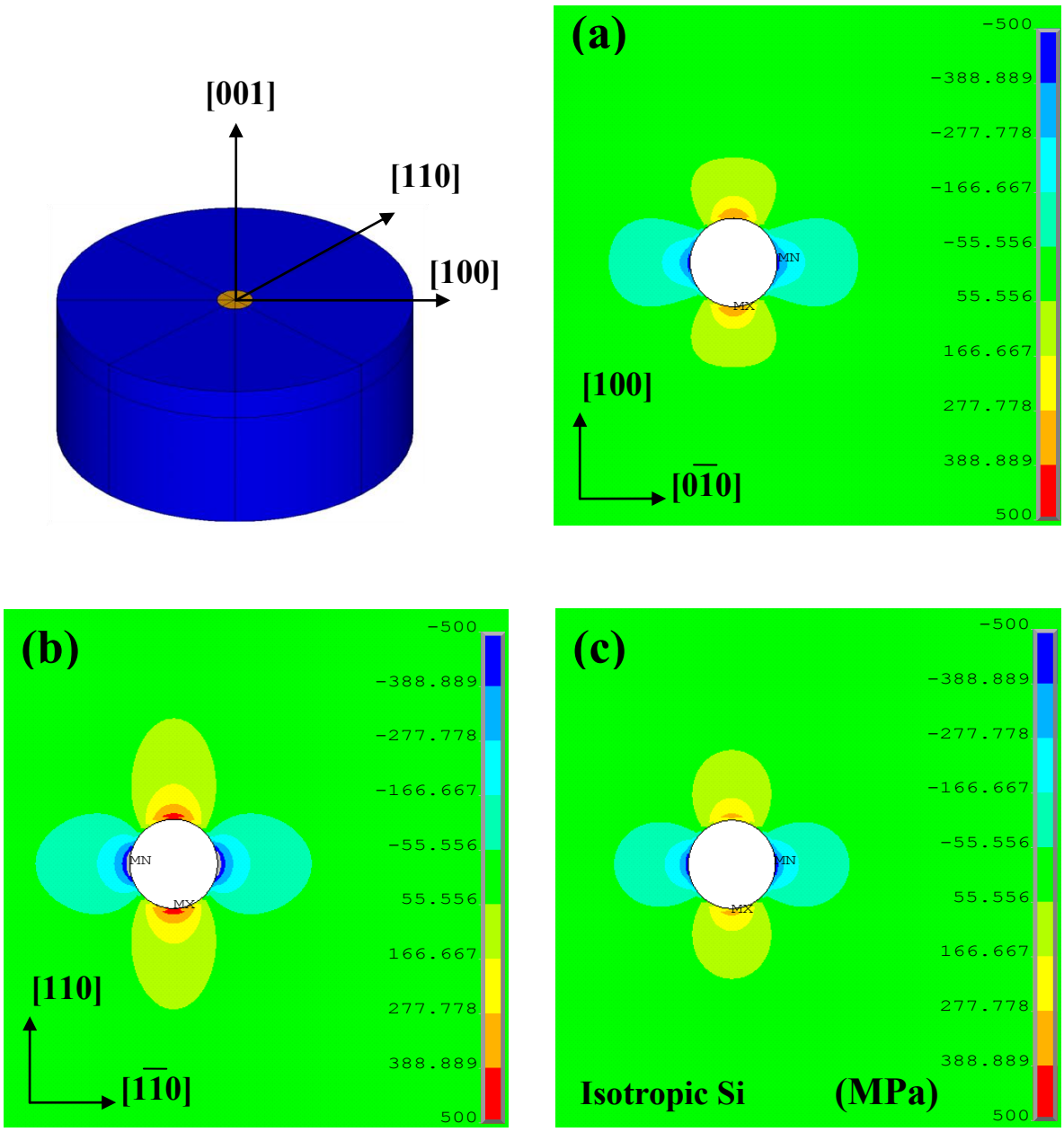


Figure 3.8: Thermal stress distribution on the Si wafer surface: (a) σ_{xx} with x axis along [100] crystal direction; (b) σ_{xx} with x axis along [110] crystal direction; (c) σ_{xx} on an isotropic Si wafer. (D_f= 20 μm, ΔT = −200 ºC)

In Figure 3.8, it is apparent that the anisotropy of Si substrate alters the thermal stress distribution on the wafer surface. Comparing Figure 3.8a to 3.8b, the magnitude and the distribution of the normal stress σ_{xx} depend on how the principle axes are defined. If the x axis is aligned with the [110] crystal direction, the intensity of σ_{xx} is increased. This is attributed to a maximum Young's modulus along [110] on a (001) Si plane [27]. Because the channel direction of MOSFET devices are always aligned along [110] crystal direction, the thermal stresses as well as the resulting KOZ are expected to be larger than that on an isotropic Si. The effect of Si anisotropy on the KOZ will be further discussed in Section 3.3.7.

3.3 TSV-INDUCED PIEZORESISTIVITY EFFECT ON MOSFETS

This section investigates the piezoresistivity effect on MOSFETs induced by the near-surface stresses surrounding TSVs. First, the piezoresistivity effect in Si is briefly reviewed in Section 3.3.1, where a stress-to-resistivity equation is introduced. Then, in Section 3.3.2, TSV-induced resistance change in Si is calculated using the equation and the FEA stress analysis. Such a resistance change calculation provides a basis for the KOZ study from Section 3.3.3 through Section 3.3.6, where the effects of TSV scaling, dielectric liner, metallization materials, and annular TSV structures are investigated. For simplicity, the Si substrate is assumed to be of elastic isotropy from Section 3.3.3 through Section 3.3.6. In the last, the effect of elastic anisotropy on KOZ is examined for a (001) Si substrate in Section 3.3.7.

3.3.1 Piezoresistivity of silicon and the keep-out zone (KOZ)

Piezoresistivity of Si refers to the effect of stresses on the mobility of the charge carriers in Si. Specific stress characteristics are commonly used to promote the performance of Si MOSFETs, and such "strained-Si" technology has been implemented in manufacturing of high-performance microprocessors since the 90-nm technology node in 2002 [40]. For this purpose, Ge is implanted into the source/drain region on a Si substrate for the p-MOS devices, and a tensile silicon nitride capping layer is applied for the n-MOSFETs [40],[41]. These processes induce a uni-axial residual stress in the middle of the respective device channel, which can enhance the carrier mobility by 35% for the n-MOSFETs and 90% for the p-MOSFETs for the 65-nm technology node [41].

The incorporation of TSV can introduce undesirable stresses in the Si matrix, which alter the performance of the adjacent MOSFETs. As illustrated in the previous section, a Cu TSV of 20 μm diameter can induce a thermal stress greater than 100 MPa at a distance 10 μm-away from the TSV edge. Stresses of such magnitude can affect the carrier mobility and will have to be taken into account in the design of the keep-out zone (KOZ). To design the KOZ, thermal stress-induced piezoresistivity effects on the carrier mobility for the MOSFETs and its distribution around the TSV have to be considered. This effect has been recently reviewed [41]. In a Si substrate, the general relations between the electric filed *E*, current density *J*, and the stress σ components can be expressed as [41]:

$$\begin{aligned}
\frac{\Delta E_1}{\rho} &= \left[\pi_{11}\sigma_1 + \pi_{12}\left(\sigma_2 + \sigma_3\right)\right]J_1 + \left(\pi_{44}\sigma_6\right)J_2 + \left(\pi_{44}\sigma_5\right)J_3, \\
\frac{\Delta E_2}{\rho} &= \left[\pi_{11}\sigma_2 + \pi_{12}\left(\sigma_1 + \sigma_3\right)\right]J_2 + \left(\pi_{44}\sigma_6\right)J_1 + \left(\pi_{44}\sigma_4\right)J_3, \\
\frac{\Delta E_3}{\rho} &= \left[\pi_{11}\sigma_3 + \pi_{12}\left(\sigma_1 + \sigma_2\right)\right]J_3 + \left(\pi_{44}\sigma_5\right)J_1 + \left(\pi_{44}\sigma_4\right)J_2,
\end{aligned} \tag{3.7}$$

where ρ is the resistivity of the unstrained Si. π_{11}, $\pi_{12,}$ and π_{44} are the piezoresistivity coefficients of Si. The subscripts of *E* and *J* (1, 2, and 3) designate the components along the three <100> crystal axes, while the subscripts of σ designate the six independent components of the stress tensor with $\sigma_1 = \sigma_{xx}$, $\sigma_2 = \sigma_{yy}$, and so on.

Consider first the case where a MOSFET is located on a (001) Si wafer with its channel direction aligned along the [100] direction (Figure 3.9a). Assume that the electrical current only flows along the channel direction, i.e. $J_2 = J_3 = 0$, and only the electric field across the channel (ΔE_1) is measured. The average resistivity (or mobility) change along the channel direction can be deduced from Equation 3.7:

$$\frac{\Delta\rho_1}{\rho} = \frac{\Delta\mu_1}{\mu} = \pi_{11}\sigma_1 + \pi_{12}(\sigma_2 + \sigma_3), \tag{3.8}$$

The channel direction of a MOSFET is often aligned along the [110] direction on a (100) wafer (Fig. 3.9b). In this case, the resistivity or the mobility change in Equation 3.8 can be deduced by rotating the coordinate system as [41]:

$$\begin{aligned}
&\frac{\Delta\rho_{1'}}{\rho} = \frac{\Delta\mu_{1'}}{\mu} = \pi'_l\sigma_{1'} + \pi'_t(\sigma_{2'} + \sigma_{3'}),\\
&\pi'_l = \frac{\pi_{11} + \pi_{12} + \pi_{44}}{2},\\
&\pi'_t = \frac{\pi_{11} + \pi_{12} - \pi_{44}}{2},
\end{aligned} \tag{3.9}$$

where σ' are the stress components in the new coordinate system, which is illustrated by red dash lines in Figure 3.9b. π'_l and π'_t are the longitudinal and transverse piezoresistive coefficients of the new channel direction, respectively. Figure 3.10 shows the graphic representations of the variations of the longitudinal and transverse piezoresistive coefficients with the channel directions on the (001) surface in p- and n-Si [41],[42].

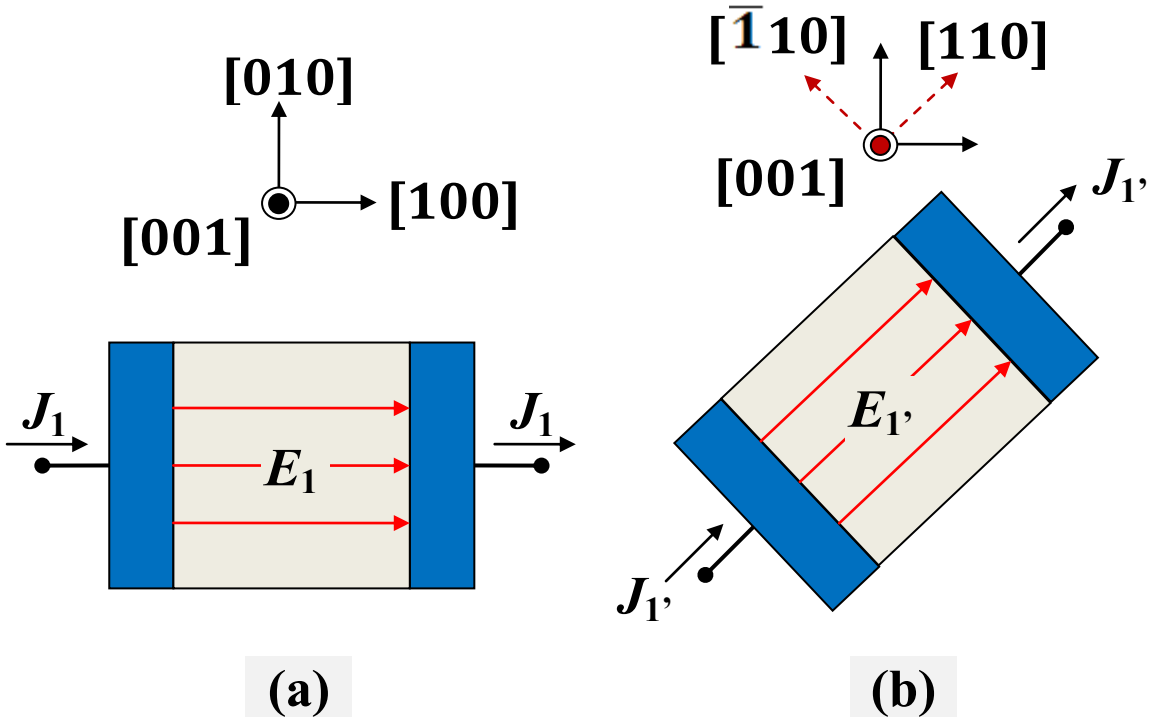


Figure 3.9: Channel direction of MOSFETs on (001) Si wafer. (a) Channel aligned with [100] crystal direction; (b) Channel aligned with [110] crystal direction. (Source: Sun in Ref. [41]; this diagram is redrawn by the author)

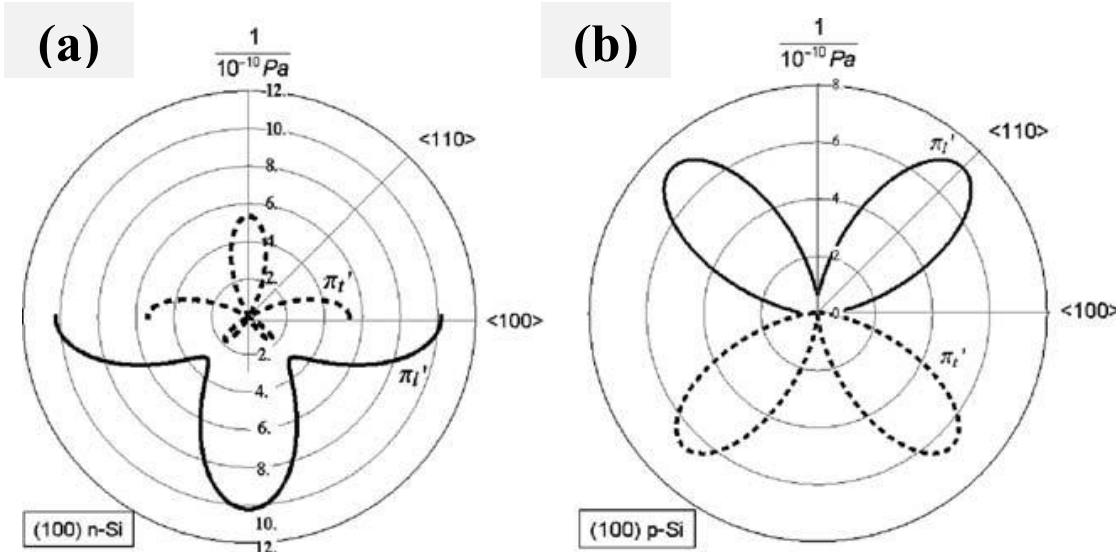


Figure 3.10: Longitudinal and transverse piezoresistive coefficients on (001) Si wafer. (a) Coefficients for n-MOSFETs on (001) Si wafer; (b) Coefficients for p-MOSFETs on (001) Si wafer. (Source: Kanda in Ref. [42])

Because the MOSFETs are usually fabricated very near the wafer surface, the out-of-plane stress component $\sigma_{3'}$ is about two orders of magnitude smaller than the in-plane component $\sigma_{2'}$ and thus is negligible in Equation 3.9. Additionally, it is clear from Equation 3.8 and 3.9 that the shear stress components ($\sigma_{4'}$, $\sigma_{5'}$ and $\sigma_{6'}$) do not contribute to the mobility change. Therefore, the distribution of the KOZ is mainly controlled by the in-plane normal stresses parallel and perpendicular to the channel direction of MOSFETs. The distribution of normal stresses on the wafer surface is two-

fold rotational symmetric (Figure 3.5 and 3.8). Consequently, the distribution of the mobility change (or the KOZ) should have a two-fold rotational symmetry as well.

3.3.2 Finite element analysis of the mobility change

To calculate the mobility change induced by an isolated TSV, thermal stress analysis is first performed using FEA simulation. The simulation procedure is similar to that described in Section 3.2.4, except that the Si substrate is assumed to be elastically isotropic for simplicity. The FEA model consists of a quarter of a TSV embedded in a Si matrix with a TSV diameter D_f of 20 μm and wafer thickness of 100 μm. The TSV material is taken to be Cu, and the material properties used in FEA simulation are listed in Table 3.1. A negative thermal load, $\Delta T = -180^{o}C$, is applied and the thermal stresses are calculated. Since the devices are fabricated very near the Si surface, the normal stresses (σ_{xx}, σ_{yy}, and σ_{zz}) are simply taken to be on the wafer surface (z = 0) from the simulation results and substituted into Equation 3.9. In the mobility change calculation, the channel direction of MOSFETs is assumed to be parallel to [110] direction, and the piezoresistivity coefficients of bulk n-Si and p-Si (Table 3.2) are used.

Table 3.2: Piezoresistivity coefficients for bulk Si (10^{-4} MPa^{-1}) (Source: Smith [43])

	π_{11}	π_{12}	π_{44}	$\frac{\pi_{11} + \pi_{12} + \pi_{44}}{2}$	$\frac{\pi_{11} + \pi_{12} - \pi_{44}}{2}$
Direction	π // [100]	$\pi \perp$ [100]		π // [110]	$\pi \perp$ [110]
n-Si	-10.22	5.37	-1.36	-3.16	-1.76
p-Si	0.66	-0.11	13.81	7.18	-6.63

The results obtained for the mobility changes along the [110] channel direction are shown in Figure 3.11, revealing a significant difference of the stress effect on the carrier mobility for the n- and p-MOS devices. With the same TSV geometry and thermal load (-180^{o}C), the maximum mobility change can reach 35% for the p-MOSFET while it is only 7% for the n-MOSFET. The result can be attributed to the combination of the sign and magnitude of the stresses and the piezoresistivity coefficients for these two types of devices. First, TSV-induced in-plane normal stresses (σ_{xx} and σ_{yy}) are of similar magnitude but are opposite in sign. Second, the piezoresistivity coefficients parallel and perpendicular to [110] crystal direction are opposite in sign for p-Si (7.18 v.s. -6.63 *10^{-4} MPa^{-1}), but of the same sign for n-Si (-3.16 v.s. -1.76 *10^{-4} MPa^{-1}). This results in an addition of the contributions from σ_{xx} and σ_{yy} for the p-MOSFET, but a subtraction of the contributions from σ_{xx} and σ_{yy} for the n-MOSFET.

If the channel direction is along the [100] direction, the piezoresistivity effect would be quite different. Here the piezoresistivity coefficients for n-Si along the parallel and perpendicular directions are opposite in sign (-10.22 v.s. 5.37 *10^{-4} MPa^{-1}),

and are an order of magnitude larger than that for p-Si (0.66 v.s. -0.11 $*10^{-4}$ MPa^{-1}). Consequently, n-MOSFETs along the [100] direction are more sensitive to the TSV-induced thermal stresses than p-MOSFETs.

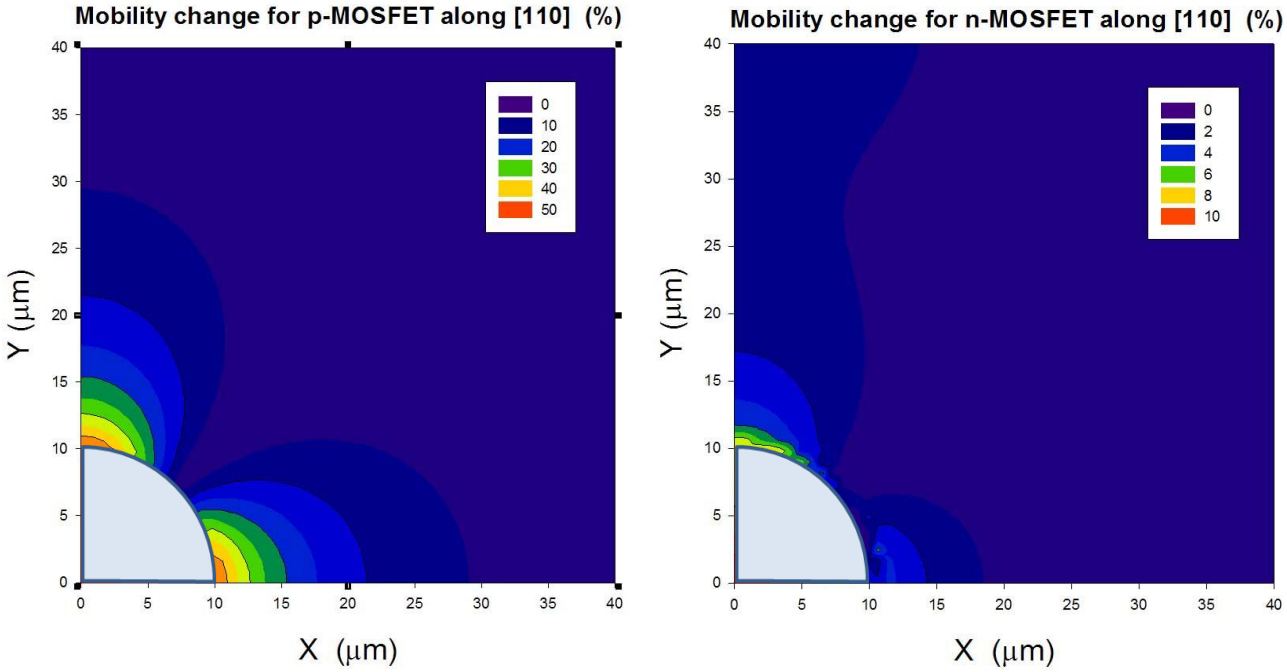


Figure 3.11: Distribution of mobility change for p- and n-MOSFETs along [110] crystal direction on a (001) Si substrate. The elastic anisotropy of Si is ignored for simplicity. (D_f = 20 μm, ΔT = −180 ºC)

3.3.3 Scaling effect of TSV on KOZ: TSV diameter and wafer thickness

The diameter of TSV used in 3-D integration, depending on the integration strategy, can range from 100 micron to only a few microns. The thickness of the Si wafer (or the height of TSV) usually ranges from 200 micron to 25 micron [1]. Scaling down the diameter and the height of TSV can increase the density of interconnects, and reduces the packaging form factor. However, there are manufacturing problems caused by the scaling of the TSV dimensions, such as metal-filling for high aspect-ratio TSVs and handling of ultra thin Si wafers. In addition, there are reliability concerns coming with TSV scaling.

It is clear that scaling of TSV can affect the thermal stress distribution and the design of the KOZ. The effect of TSV diameter on thermal stress can be seen from Equation 3.1 and 3.2. To understand the scaling effect on KOZ, the mobility change induced by TSVs is investigated as a function of TSV diameter and height, following the procedure described in the previous section. For this purpose, FEA models of Cu TSVs are built with a fixed wafer thickness (100 μm) and varying diameter (D_f = 10 ~ 30 μm). This is combined with models where the TSV diameter D_f is fixed at 20 μm but with varying TSV height (H = 20 ~ 200 μm). A negative thermal load, $\Delta T = -180^{o}C$, is applied to all models. The channel direction is assumed to be along [110] crystal direction. After calculating the mobility change on the wafer surface for both p-Si and n-Si, an arbitrary criterion for KOZ equivalent to 10% change in mobility is applied to calculate the area of KOZ surrounding the TSV. The results are plotted in Figure 3.12 and 3.13 for the p-MOSFET devices.

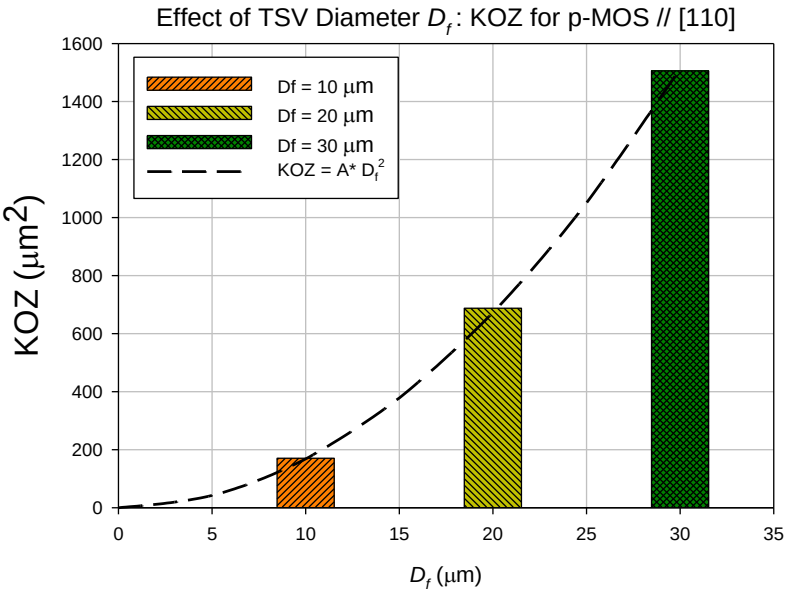


Figure 3.12: Effect of TSV diameter on KOZ for p-MOSFETs along [110] crystal direction. (D_f= 20 μm, ΔT = −180 ºC)

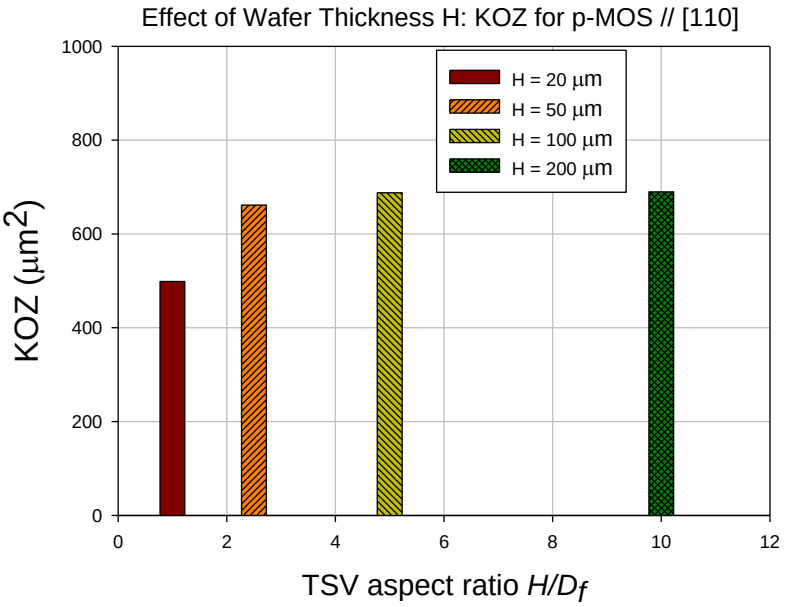


Figure 3.13: Effect of wafer thickness on KOZ for p-MOSFETs along [110] crystal direction. (D_f= 20 μm, ΔT = −180 ºC)

The effect of TSV diameter D_f on KOZ shown in Figure 3.12 indicates a significant effect on the area of KOZ for p-MOSFET, increasing approximately with the square of D_f. Overall, the effect yields an area ratio between KOZ and TSV of about 2. It is interesting to note that the TSV-induced stresses cannot generate a mobility change greater than the 10% criterion in n-MOSFET under the given thermal load (-180^{o}C), therefore, there is no KOZ needed for n-MOSFETs along [110].

The effect of wafer thickness is shown in Figure 3.13. The area of KOZ for p-MOSFET initially increases with the wafer thickness H, and then reaches a stable value after the wafer thickness is greater than $5D_f$. This is because the thermal stress distribution on the wafer surface stabilizes when the bottom surface is far away from it. For a thin TSV wafer, the thermal stresses will be less on the wafer surface, resulting in a smaller KOZ.

3.3.4 Effect of dielectric liner on KOZ

During the fabrication of Cu TSVs, dielectric liners and barrier layers are deposited on the via side wall before Cu electroplating. The dielectric layer, which is often made of 1~2 μm thick of silicon oxide, insulates the TSV from the Si substrate. Between the dielectric liner and the Cu TSV, a barrier layer is coated to protect the Si from Cu diffusion, and to promote the adhesion between the dielectric liner and the Cu. Barrier layers are usually made of metallic materials such as Ti, Ta, and TiN, with a thickness less than 0.1 μm [10], [44], [45]. Because the thickness of the barrier layer is

much less than the dimension of Cu TSV, thermal stress induced by such barrier layers can be neglected.

In addition to silicon oxide-based dielectric, polymeric materials such as parylene or BCB (benzocyclobutene) have been used to replace the oxide dielectric and the barrier layers [7], [8]. Compared to silicon oxide, BCB is softer in modulus (3 GPa) and has a lower dielectric constant. The advantages of using a 2~5 μm thick polymer liner include lower stresses in the TSV structure and less capacitance in the interconnects. It has been reported that a soft polymer liner can reduce the thermal stress and the risk of silicon cracking [46], and the electrical performance can be improved by reducing the capacitive coupling [8].

The effect of dielectric liner on KOZ is investigated for both silicon oxide and BCB materials. FEA simulations are conducted for 20 μm Cu TSVs with a 1~2 μm thick of dielectric layer between Cu and Si. A negative thermal load $\Delta T = -180^{o}C$ is applied to all models. The mobility change in p-MOSFETs on a (001) Si wafer is calculated, and the channel direction is assumed to be along [110] crystal direction. The criterion of 10% mobility change is again applied to calculate the area of KOZ. The results are shown in Figure 3.14.

The area of KOZ is compared for several scenarios in Figure 3.14. The red bars represent the KOZ calculated using the 10% mobility change criterion, while the orange bars represent the area occupied by the dielectric liner. For TSVs with a TEOS oxide liner, the reduction in KOZ due to the stress-buffering is compensated by the area of liner, resulting in a minimum difference in KOZ from a TSV without liner. On the other hand, the stress-buffering by a BCB liner significantly reduces the area of KOZ by ~40%. The effect of liner thickness on KOZ is not significant for both types of dielectrics in this study.

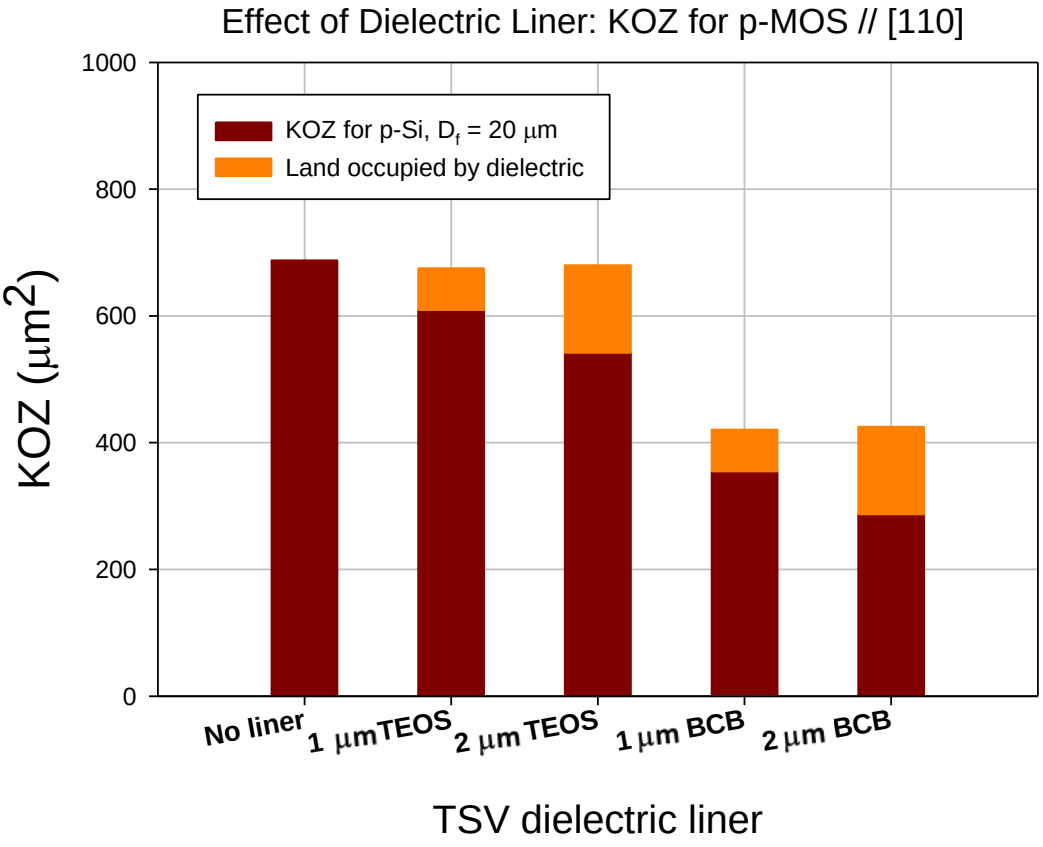


Figure 3.14: Effect of dielectric liner on KOZ for p-MOSFETs along [110] crystal direction. (D_f= 20 μm, ΔT = −180 ºC)

3.3.5 Effect of metallizations on KOZ

As an alternative to Cu TSVs, several metallization materials including aluminum (Al), nickel (Ni), and tungsten (W) have been considered. The effect of materials on KOZ is evaluated using the thermo-mechanical properties listed in Table 3.1. The areas of KOZ for the four TSV materials of the same TSV diameter (20 μm) are compared in Figure 3.15 under the same thermal load (-180ºC). Compared to Cu, Al has a larger

mismatch in thermal expansion with Si. As a result, the thermal stresses as well as the KOZ are both larger for Al under the same thermal load. In contrast, Ni has a higher Young's modulus than Cu but a lower thermal mismatch, resulting in a smaller KOZ. Despite having the highest Young's modulus, W has the least CTE mismatch with Si among these four materials. The mobility change is less than 10% even for p-MOSFETs, and thus no KOZ is required for W TSV. This renders W an attractive metal for TSV fabrication. However, the deposition of W requires a higher process temperature (450°C) than that of Cu and Ni, which can induce a larger residual stress in W TSVs [12]. Therefore, the difference in process temperatures needs to be considered for a more precise comparison in KOZ.

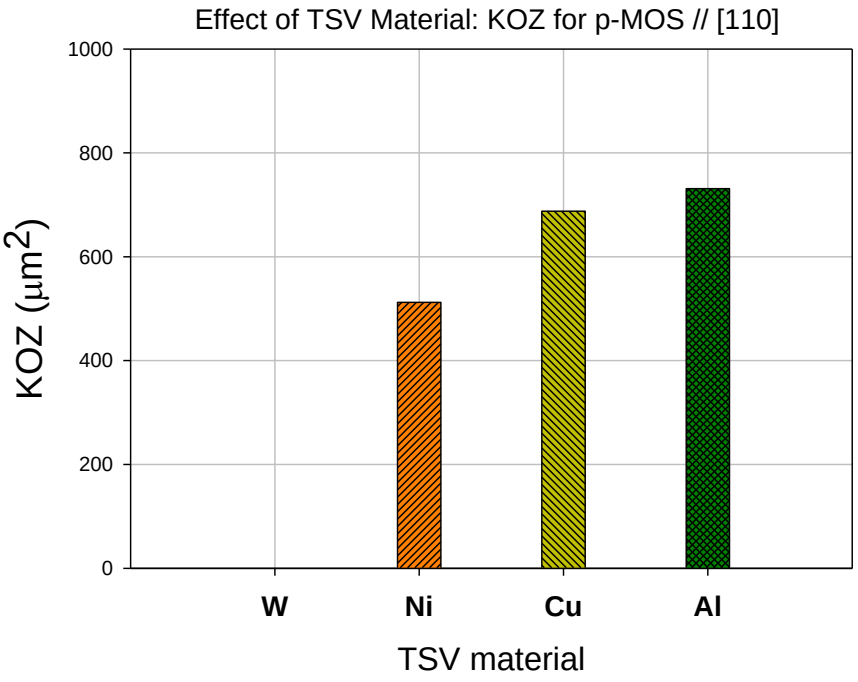


Figure 3.15: Effect of TSV metallization materials on KOZ for p-MOSFETs along [110] crystal direction. (D_f = 20 μm, ΔT = −180 ºC)

3.3.6 Effect of TSV geometry: annular TSVs

Various TSV geometry designs have been introduced to improve the thermo-mechanical reliability of the interconnect structures [31],[47]. Among them, the annular TSV structure has been reported to reduce the thermal stresses in Si substrate and at the TSV/Si interface [46],[48]. Consider an annular TSV embedded in a Si substrate with an inner-diameter D_i and outer-diameter D_f under a thermal load ΔT (See illustration in Figure 3.16). The thermal stresses in Si can be expressed using a 2-D plane-strain solution [48]:

$$\sigma_r^{Si} = -\sigma_\theta^{Si} = \frac{-E\ \varepsilon_T}{2(1-\nu)}\left(\frac{D_f}{2r}\right)^2\left(1-\eta^2\right), \quad \eta = \frac{D_i}{D_f} \tag{3.10}$$

where η is the ratio of the inner- to outer-diameter of the annular TSV, and the elastic mismatch between TSV and Si is ignored for simplicity. According to Equation 3.10, it is apparent that the magnitude of both radial and circumferential stresses in Si reduces with increasing D_i. Therefore, it is expected that the annular structure can also reduce the KOZ on the Si wafer surface.

The effect of annular structure on KOZ is examined using FEA simulation. FEA models of annular TSVs are constructed with a fixed outer-diameter (20 μm) and varying inner-diameter (D_i = 0 ~ 15 μm). A negative thermal load ΔT = -180^{o}C is applied to all models. The KOZ for p-MOSFETs // [110] on a (001) Si wafer surface is again calculated using the 10% mobility change criterion. The results are plotted in Figure 3.16.

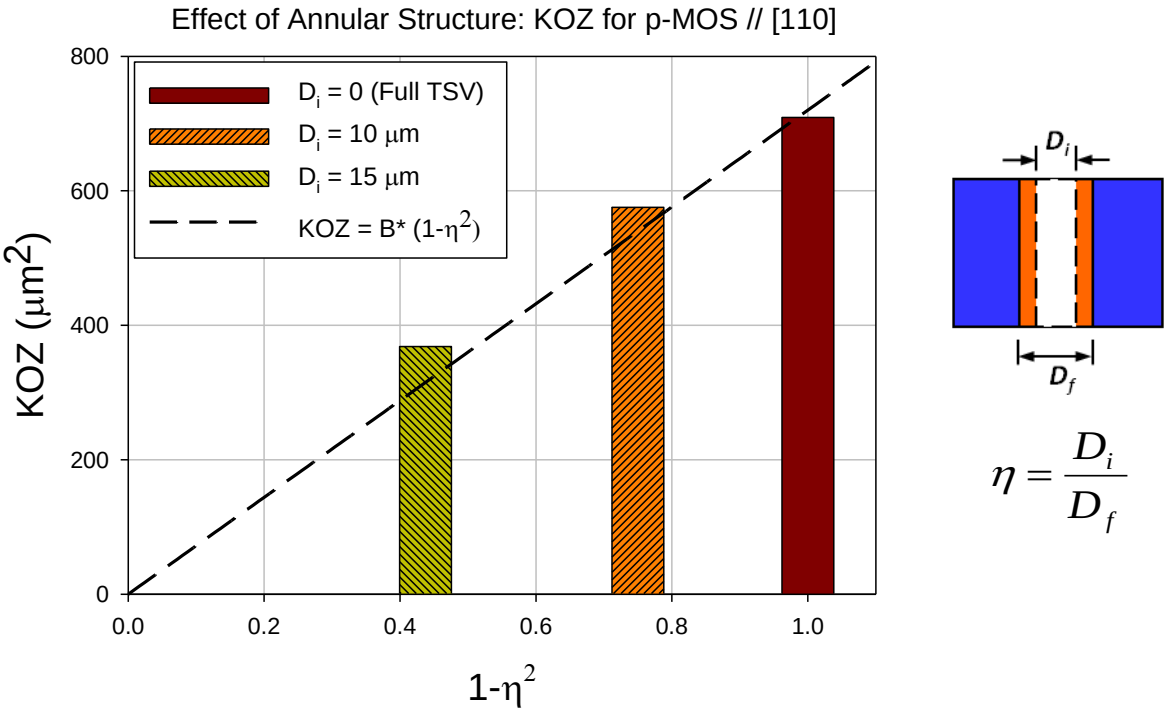


Figure 3.16: Effect of annular TSV structure on KOZ for p-MOSFETs along [110] crystal direction. (D_f = 20 μm, ΔT = −180 ºC)

In Figure 3.16, the area of KOZ reduces with increasing D_i. Comparing the annular TSV with D_i = 15 μm to the fully filled TSV (D_f = 20 μm), The KOZ is smaller by ~50%. The KOZ will vanish when the inner-diameter approaches the outer-diameter (i.e. an empty TSV hole with $1-\eta^2 = 0$). Another observation is that the area of KOZ is roughly proportional to $1-\eta^2$, as indicated by the black dashed line in Figure 3.16.

3.3.7 Effect of Si anisotropy

The effect of elastic anisotropy of Si on thermal stress distribution has been previously discussed in Section 3.2.4. Here the elastic anisotropy effect on KOZ is further investigated using FEA. Following the same procedure, the area of KOZ for p- and n-MOSFETs along both [110] and [100] crystal directions are obtained using the stiffness matrix of (001) Si (Section 3.2.4). Then, the results are compared to that obtained using isotropic elastic constants of Si (i.e. E_{Si} = 130 GPa, ν_{Si} = 0.28). The comparison is shown in Figure 3.17.

As shown in Figure 3.17, the amount of mobility change is below 10% for n-MOS // [110] and for p-MOS // [100] so that the KOZ vanishes in both cases. Comparing the isotropic Si to the anisotropic Si, the elastic anisotropy increases the area of KOZ by ~6% and ~44% for n-MOS // [100] and p-MOS // [110], respectively. The elastic anisotropy of Si does affect the shape and area of KOZ, and therefore it should be considered for one to design the KOZ surrounding TSVs. However, it should be noted that the piezoresistivity anisotropy plays a more significant role than the elastic anisotropy in the determination of KOZ. For instance, the KOZ for p-MOSFETs vanishes after rotating the channel direction from [110] to [100] crystal direction. This is attributed to the fact that the piezoresistivity coefficients are highly directional-dependent on (001) Si (See Figure 3.10).

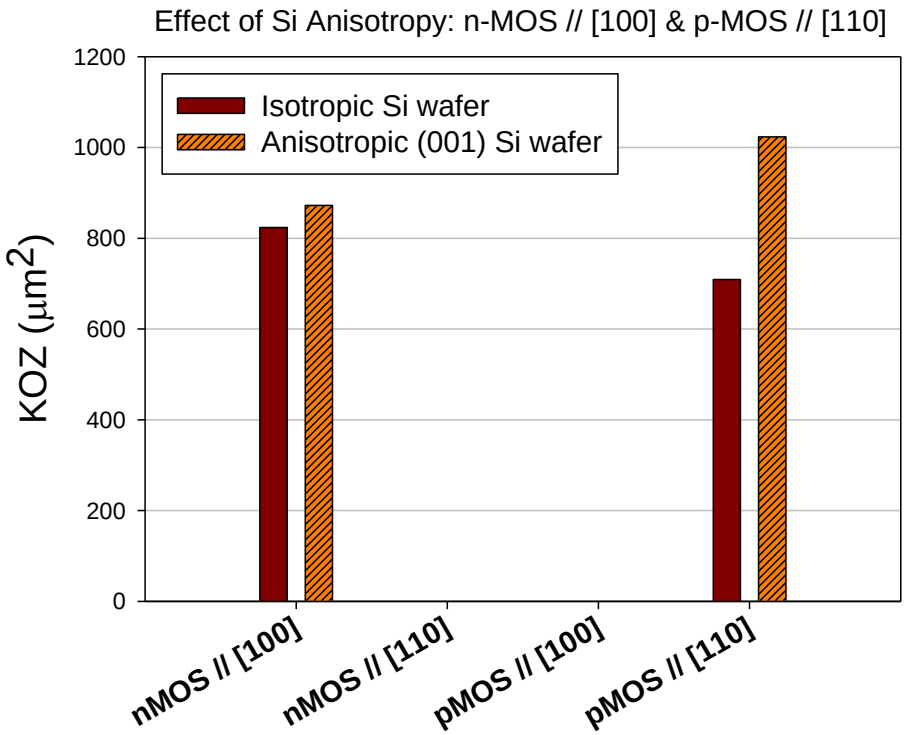


Figure 3.17: Effect of elastic anisotropy of Si on KOZ for n- and p-MOSFETs along [100] and [110] crystal directions. (D_f = 20 μm, ΔT = −180 ºC)

3.4 SUMMARY

This chapter studies the TSV-induced thermal stresses on Si wafers and the resulting piezoresistivity effect on the design of the keep-out zones (KOZ) for MOSFET devices. TSV-induced thermal stresses are investigated using FEA combined with analytical methods. The thermal stresses on Si wafers are found to depend on the thermal loading and the mismatch of thermal expansion coefficients (CTEs) between TSV and Si,

and vary with the square of the ratio between TSV diameter and the distance away from TSV. The thermal stress distribution is further examined in a Cartesian coordinate system, where a two-fold rotational symmetry of stress distribution is observed. The impact of the thermal stress on the design of keep-out zone (KOZ) is investigated by examining the stress-induced piezoresistivity effect on the carrier mobility of MOSFET devices. A criterion based on a 10% change in carrier mobility is used to define the area of the KOZ for both p- and n-MOSFETs. The analysis indicates that the area of KOZ can be controlled by optimizing the thermal loading, TSV diameter, wafer thickness, the metallizations of TSVs, and TSV geometry such as annular structures. Finally, the effect of elastic anisotropy of Si on KOZ is examined. The elastic anisotropy can impact the thermal stress distribution as well as the amount of KOZ. Consequently, the elastic anisotropy of Si should be considered in designing the KOZ for MOSFET devices.

Chapter 4: Thermal Stress-Induced Delamination of TSVs

4.1 INTRODUCTION

Inside TSV infrastructures, thermal stresses exist ubiquitously owing to the CTE mismatch between the metallic materials in the TSV and the Si matrix. Thermal stresses in the Si matrix can impact the electrical performance of the semiconductor devices, which has been discussed previously in Chapter 3. Thermal stresses can also develop near the interface between the TSV and Si, causing interfacial delamination of the TSV as well as fracture in the interconnect structure [18]. In fact, such thermal stress-induced TSV delamination has been found to be one of the dominant failure modes for 3-D interconnects. Once delaminated, TSVs can protrude from the Si wafer and therefore damage the interconnect structures [17]. In order to investigate the TSV delamination under thermal loadings, finite-element-analysis (FEA) has been applied to simulate the driving force for TSV delamination. In general, the crack driving force was found to increase with the diameter of TSVs and the length of circumferential crack [18][49].

In this chapter, the driving force and the delamination mechanism for TSV structures are further investigated. First, the energy release rate (ERR) that drives the TSV delamination is evaluated using analytical solutions deduced for simplified TSV structures. The results are supplemented and compared with FEA simulations. This is followed by a study on the impact of structural design and metallization materials on the reliability of the TSV structure. The effect of TSV geometry is investigated and compared among four types of TSV structures: (a) fully filled TSV, (b) annular TSV, (c) TSV with a dielectric liner, and (d) TSV with an overlaying metal pad, i.e., a nail-head TSV structure (see Figure 4.1). In the last part, a TSV protrusion mechanism is proposed for a nail head TSV. The development of TSV delamination under cyclic thermal loadings will be discussed.

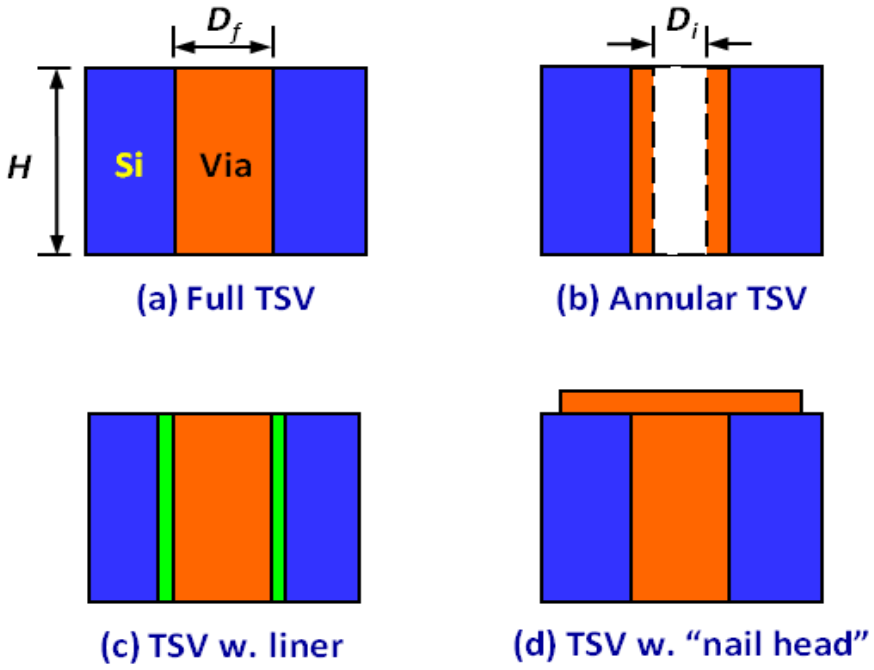


Figure 4.1: Schematics of through-silicon vias (TSVs) in various structural forms.

It should be noted that the study in this chapter is the result of active collaboration between the author and Prof. Huang's group at the University of Texas at Austin. The analytical solutions in the following sections were first derived by Prof. Huang and were further developed by Suk-Kyu Ryu, who also simulated the crack driving forces for TSV delamination using the J-integral method in the ABAQUS® software. The author's contributions include formulating the problems and reproducing some of the simulations using the ANSYS® software. Such a study has been co-published in Ref. [26], [48], and [49].

4.2 TSV DELAMINATION INDUCED BY OPPOSITE THERMAL LOADS

Thermal stresses in TSVs are induced during processing and thermal cycling. Figure 4.2 plots the distribution of thermal stresses simulated using an axi-symmetric FEA model. Here only the stress components contributing to TSV delamination are discussed (σ_{rz} and σ_{rr}). Given an arbitrary thermal load, the shear stresses σ_{rz} and the radial stress σ_{rr} are axi-symmetrically distributed, and such two stress components vary with the location on the cross-section of TSV. Consider first the effect from the shear stress σ_{rz}. The FEA results reveal a shear stress concentration around the TSV boundary near the wafer surface, where the shear stress has opposite signs depending on whether a heating or a cooling thermal load. The different signs of the shear stress will drive the copper TSV to "pop-up" or to cave in from the wafer surface. In both cases, the shear stress concentration can drive an interfacial delamination along the TSV/silicon interface with the same magnitude of the driving force.

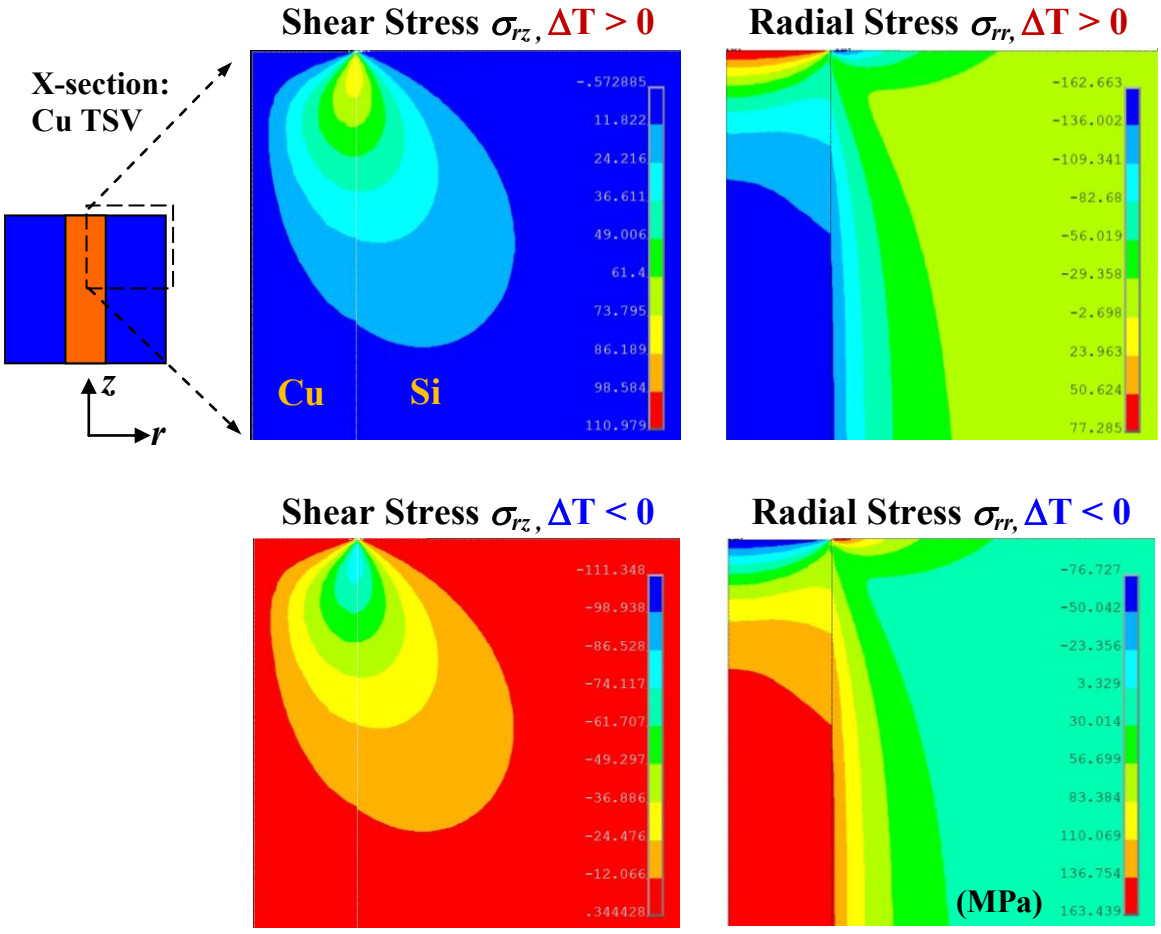


Figure 4.2: Distribution of thermal stresses σ_{rz} and σ_{rr} on the cross-section of Cu TSV under opposite thermal loads.

The radial stresses along the TSV/Si interface are also opposite in sign depending on whether a heating or a cooling thermal load is applied. In contrast, the different signs of the radial stresses induce distinct effects on interfacial delamination. Assuming the CTE of TSV is larger than that of Si, only the tensile radial stress induced by a negative thermal load ($\Delta T < 0$) can drive the TSV delamination. The compressive stress on the

TSV/Si interface induced by a positive thermal load ($\Delta T > 0$) does not contribute to the TSV delamination.

The difference between two opposite thermal loads is further illustrated in Figure 4.3. Assuming an axi-symmetric, circumferential crack initiates from the wafer surface and propagates along the TSV/Si interface. With a positive thermal load ($\Delta T > 0$), such crack is only driven by the shear stress. This results in an interfacial crack with a pure shearing mode (mode II). On the other hand, with a negative thermal load ($\Delta T < 0$), the delamination is driven by both the shear stress and the tensile radial stress. Consequently, the interfacial crack grows in a mixed mode (peeling and shearing). Given opposite but the same magnitude of thermal loads, the magnitude of the shear stresses is the same. This implies that the TSV interface is more vulnerable to cracking under a cooling condition due to an additional contribution of the tensile radial stress.

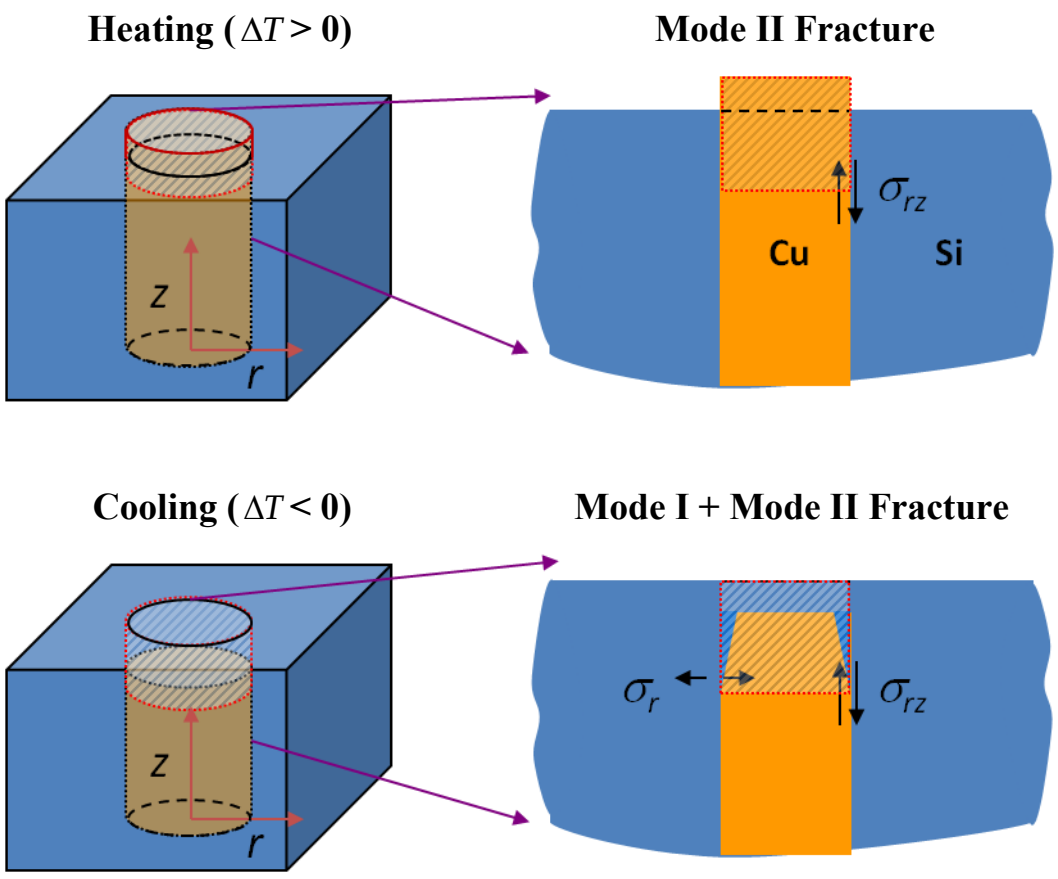


Figure 4.3: Schematics of interfacial delamination of TSV under cooling and heating conditions. In both cases, the interfacial crack is assumed to grow axi-symmetrically from one surface towards the other surface.

4.3 CRACK DRIVING FORCE FOR TSV DELAMINATION

This section investigates the driving force for TSV delamination under thermal loads. The crack driving force, as known as the energy release rate (ERR), is first derived using analytic solutions for a simplified TSV structure (Figure 4.1a). Such analytic solutions are further compared to FEA simulations in Section 4.3.2. Key parameters that control the driving force for TSV delamination are to be discussed.

4.3.1 Analytical solutions: steady-state energy release rate (ERR)

The crack driving force for a steady-state TSV delamination has been derived for both the cooling and heating conditions by Ryu et al. [26]. Consider an infinitely long fiber (TSV) in an infinite matrix (Si wafer) with a semi-infinite, circumferential crack along the TSV/Si interface. The crack tip is far away from the wafer surface so that the steady-state condition applies. Given a thermal load ΔT, the steady-state ERR (per unit area) for the interfacial crack growth can be obtained by comparing the elastic strain energy far ahead of the crack front and that far behind the crack front. The steady-state ERR per unit area, G_{ss}, can be expressed as follows [26]:

$$G_{cooling}^{SS} = \frac{E_m \varepsilon_T^2 D_f}{4}\left(\frac{(1+\nu_f)(1+\alpha_D)}{(1-2\nu_f)(1-\alpha_D)+(1+\alpha_D)\dfrac{1+\nu_m}{1+\nu_f}} + \frac{1}{2}\frac{1+\alpha_D}{1-\alpha_D} \right), \qquad (4.1)$$

$$G_{heating}^{SS} = \frac{E_m \varepsilon_T^2 D_f}{4}\left(\begin{array}{l} \dfrac{(1+\nu_f)(1+\alpha_D)}{(1-2\nu_f)(1-\alpha_D)+(1+\alpha_D)\dfrac{1+\nu_m}{1+\nu_f}} + \dfrac{1}{2}\dfrac{1+\alpha_D}{1-\alpha_D} \\ -\dfrac{(1+\alpha_D)}{(1-\nu_f)(1-\alpha_D)+(1+\nu_m)(1+\alpha_D)} \end{array} \right), \qquad (4.2)$$

where $\varepsilon_T = (\alpha_f - \alpha_m)\Delta T$ is the thermal strain, and $\alpha_D = \dfrac{\overline{E}_f - \overline{E}_m}{\overline{E}_f + \overline{E}_m}$ is the first Dundurs' parameter for elastic mismatch between the TSV and Si, with $\overline{E} = \dfrac{E}{1-\nu^2}$. The subscripts m and f stands for the matrix and the TSV, respectively. For a Cu fiber embedded in a Si matrix, the elastic mismatch $\alpha_D = -0.059$ is small and thus may be

considered negligible. By neglecting the elastic mismatch (i.e., $\alpha_D = 0$ and $\nu_f = \nu_m = \nu$), Equation 4.1 and 4.2 can be simplified as follows:

$$G_{cooling}^{SS} = \frac{E\varepsilon_T{}^2 D_f}{4(1-\nu)}, \tag{4.3}$$

$$G_{heating}^{SS} = \frac{E\varepsilon_T{}^2 D_f}{4(1-\nu)} \frac{(1+\nu)}{2}, \tag{4.4}$$

According to Equation 4.1 through 4.4, the driving force for TSV delamination are controlled by parameters such as the diameter of TSV (D_f), CTE mismatch between TSV and Si $(\alpha_f - \alpha_m)$, the thermal load (ΔT), and the elastic modulus (E). The steady-state ERR is proportional to the TSV diameter, the square of the thermal load, and the square of CTE mismatch. The ERR for TSV delamination also increases with the elastic modulus of the TSV material (E_f), as implied in Equation 4.1 and 4.2. The other observation is the difference between opposite thermal loads. Comparing Equation 4.3 to 4.4, the steady-state ERR under cooling is higher than that under heating by a factor of $\frac{2}{1+\nu}$ (i.e. a factor of 1.5 if $\nu = 0.33$). Consequently, TSV delamination is more likely to occur during the cooling processes.

4.3.2 FEA simulation: non-steady state ERR

The steady-state ERR solutions (Equation 4.1 and 4.2) apply to an infinitely long TSV with a semi-infinite, circumferential crack. For a finite-sized TSV structure with a finite interfacial crack, the ERR depends on both the crack length and the wafer thickness. Such non-steady state ERR for a finite-sized TSV is calculated using FEA simulations. The simulation procedure is described in the following.

Crack length-dependent ERR:

The ERR for TSV delamination are simulated for short cracks using the ANSYS® software. Axi-symmetric FEA models are constructed for fully-filled Cu TSVs with a circumferential crack extending from the top wafer surface, as illustrated in Figure 4.4a. The TSV diameter ranges from 5 to 20 μm, while the wafer thickness is fixed at 200 μm. A 2-D plane element (PLANE182) in the ANSYS® software is selected for simulation. The material properties for the Cu TSV and Si are listed Si in Table 4.1. Such FEA models are given a negative thermal load ΔT = -250^{o}C, and then the ERRs for delamination are simulated for increasing crack lengths using the J-integral method. The interfacial crack is opened due to the negative thermal load applied, as shown in Figure 4.4b.

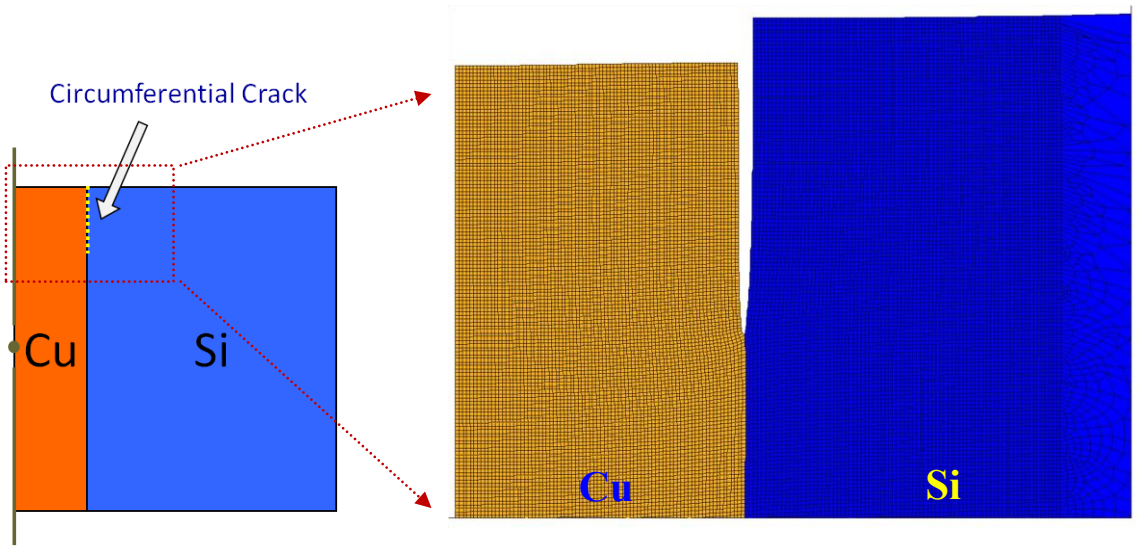


Figure 4.4: (a) Illustration of an axi-symmetric FEA model: Cu TSV with a circumferential crack between Cu/Si; (b) Element mesh near a 10 μm long interfacial crack. The crack is opened under a negative thermal load -250^{o}C (deformation scale: 20X).

Table 4.1: Thermo-mechanical properties of materials used for ERR calculation [27], [28], [36-39]

Material	CTE (ppm/K)	Young's Modulus (GPa)	Poisson's ratio
Si	2.3	130	0.28
Cu	17	110	0.35
Al	20	70	0.35
Ni	13	207	0.31
W	4.4	400	0.28
BCB	40	3	0.34

The FEA-simulated ERRs are plotted as a function of the crack length for various TSV diameters in Figure 4.5. The steady-state ERRs from Equation 4.1 are superimposed to the figure as dash lines. It is clearly observed that the ERR increases with the interfacial crack length, a, and approaches the steady-state ERR solution at a crack length $a > 2D_f$. The figure also shows that the ERR increases with the TSV diameter, and can exceed 10 J/m^2 for a TSV with 20 μm diameter under a -250°C of thermal load. By comparing the crack length-dependent ERR, $G(a)$, to the interfacial adhesion energy, Γ, a critical crack length a_c may be determined. An interfacial crack with a length beyond a_c will grows unstably under the prescribed thermal load. For a conservative design, it is required to have $G_{SS} \leq \Gamma$ so that all cracks can remain stable under thermal loading.

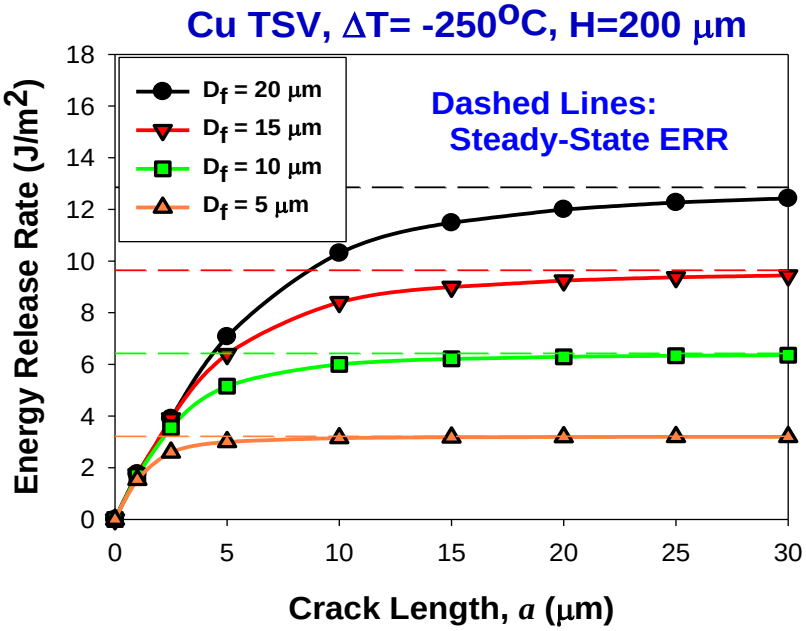


Figure 4.5: Energy release rate vs. crack length at circumference of Cu TSV for various TSV diameters. Dashed lines indicate the steady-state ERRs (ΔT= -250 ºC) [26].

Wafer thickness-dependent ERR:

To investigate the effect of wafer thickness, FEA simulations are performed on TSVs of different wafer thickness H, with the same via diameter (20 μm) and the same thermal load (-250°C). Figure 4.6 shows the ERR as a function of the crack length for various wafer thicknesses. For a relatively thin wafer, the ERR for interfacial delamination reaches a maximum at a crack length $a \sim 0.3H$, and then decreases as the crack tip approaches the other side of the wafer. The maximum energy release rate decreases as the wafer thickness decreases. Therefore, the interfacial reliability of TSVs may be improved by using thinner wafers, although other effects such as wafer handling and Si cracking may limit the minimum wafer thickness.

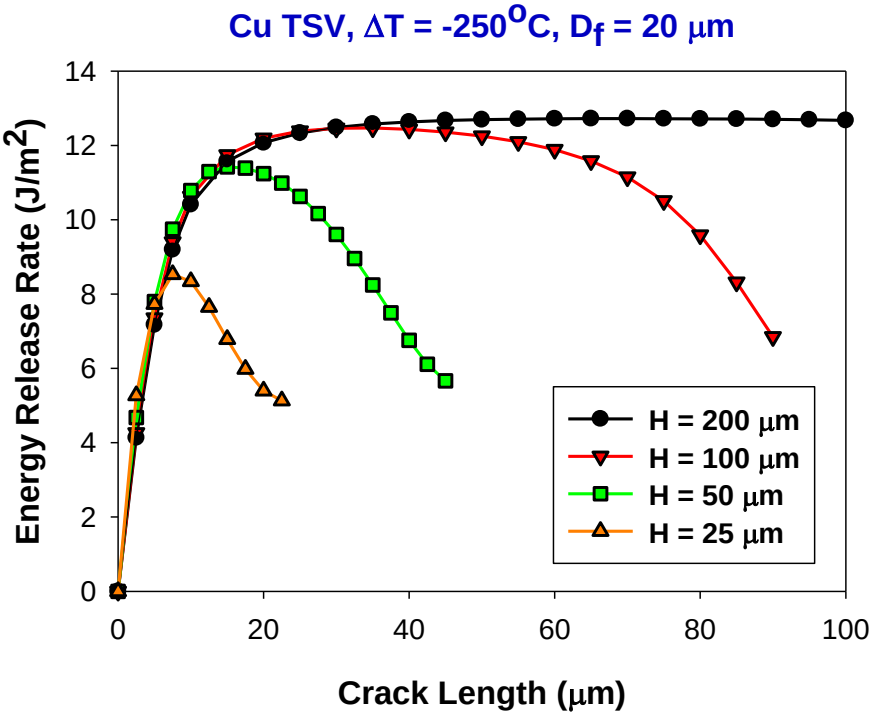


Figure 4.6: Effect of wafer thickness on the energy release rate for interfacial delamination of fully filled TSVs (D_f = 20 μm, ΔT = −250 °C) [26].

4.4 EFFECT OF TSV METALLIZATION ON DELAMINATION

Currently, TSVs in the 3-D infrastructure are fabricated with various metals, such as copper, tungsten, and nickel. The difference in thermo-mechanical reliability among these materials is of interest. Based on the steady-state ERR equations, a metal with a low modulus and a low CTE is favored for reducing the driving force for delamination. Unfortunately, a metal with low modulus usually comes with a high CTE, and vice versa. The thermo-mechanical properties of four commonly used metals are listed in Table 4.1, in which aluminum has the lowest modulus while tungsten has the smallest CTE. To compare these four materials, the ERRs for TSV delamination have been calculated for the same TSV diameter and thermal loads using Equation 4.1 and 4.2. The results are plotted in Figure 4.7.

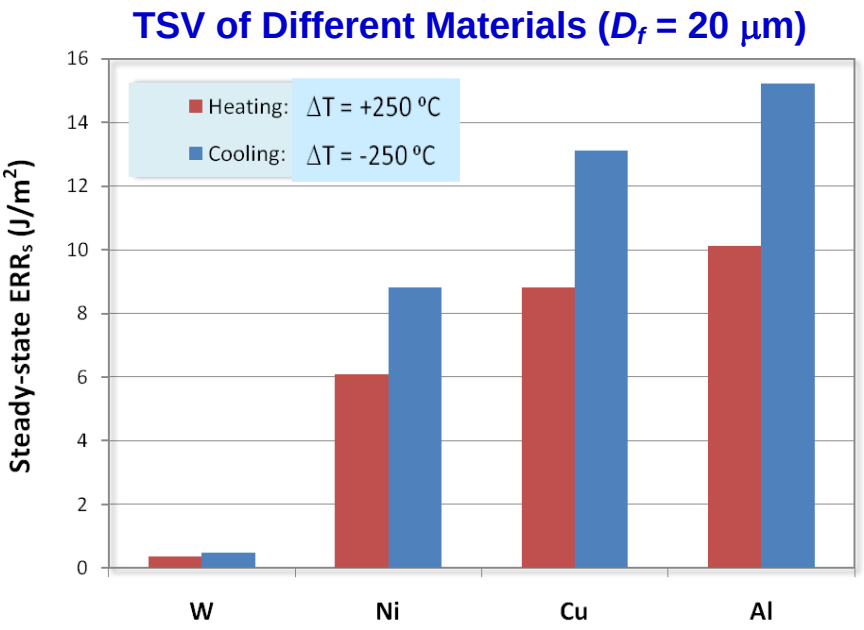


Figure 4.7: Steady-state ERRs for TSVs fully filled with four kinds of metals: tungsten, nickel, copper, and aluminum [26].

Figure 4.7 indicates that the driving force for TSV delamination significantly decreases with reduced CTE of the metal. This can be attributed to the fact that ERR is proportional to the square of the CTE mismatch between the metal and the silicon matrix. Tungsten, which has the lowest CTE among the four materials, exhibits the lower ERR for delamination. However, the tendency to delamination cannot be judged by the crack driving force alone. Processing temperatures and the interfacial adhesion between the metallization material and the barrier layer of TSVs play important roles in controlling the delamination. In this case, copper can develop more plastic deformation compared with tungsten. Therefore, copper can absorb more energy by plastic deformation near the crack tip and increase the fracture resistance to crack propagation [11]. To further compare the risk of delamination among TSV materials, adhesion measurements using experimental methods are required.

4.5 EFFECT OF TSV STRUCTURE ON DELAMINATION

The present study has considered a much simplified structure with a single TSV embedded in Si (Figure 4.1a). In practice, TSVs with annular metal filling (Figure 4.1b) have been designed and implemented in 3-D integration [50][51][31]. Moreover, a dielectric liner may be needed between the TSV and Si (Figure 4.1c), and an overlaying metal pad is usually required to form an electrical interconnect (Figure 4.1d). The effect of aforementioned TSV structures on the interfacial crack driving force is investigated in this section.

4.5.1 Annular TSV

Annular metal filling structures have been proposed for applications such as TSVs in Si interposers. The plating time and cost can be both reduced by partially filling the vias. In addition, it has been reported that the annular TSV design can reduce the thermal stresses in Si and therefore enhance the thermo-mechanical reliability [31][52].

The annular TSV design can also reduce the driving force for TSV delamination. The steady-state energy release rate for delamination in annular TSVs has been derived for the cooling conditions by Ryu et al. [26]. By ignoring the elastic mismatch between TSV and the matrix for simplicity, the steady-state ERR, G_{ss}, can be expressed as:

$$G_{SS} = \frac{E\varepsilon_T{}^2 D_f}{4(1-\nu)}\left(1-\eta^2\right), \qquad \eta = \frac{D_i}{D_f} \tag{4.5}$$

where η represents the ratio of the inner- to the outer-diameters of an annular TSV. According to Equation 4.5, the ERR decreases significantly with decreasing metal thickness in the annular TSV. For a very thin layer of metallization, delamination energy can reduce to nearly zero. This suggests that the driving force for TSV delamination can be effectively reduced using an annular structural design.

The steady-state ERR solution for annular structures is compared with FEA simulations. Axi-symmetric FEA models are constructed for annular Cu TSVs using a similar procedure as described in Section 4.3.2. The inner diameter D_i ranges from 5 μm to 15 μm while the outer diameter is fixed at 20 μm. The non-steady state ERR for TSV delamination is simulated for a -250^{o}C of thermal load. Figure 4.8 shows a good

agreement between the steady-state solution and the FEA simulations for a long crack length. The results also indicate that the thinner the annular metal, the shorter the crack length to reach the steady-state.

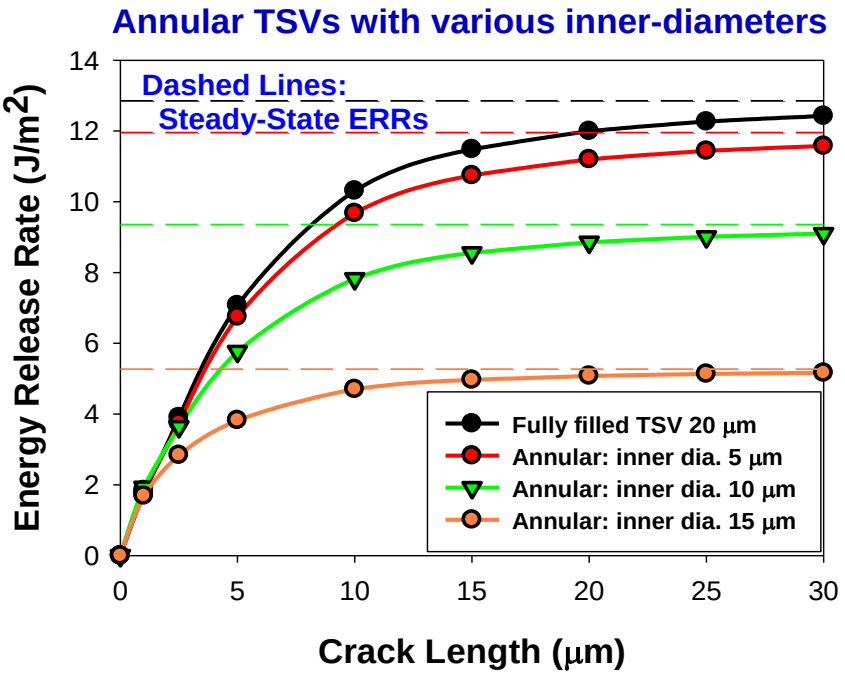


Figure 4.8: FEA-simulated ERRs for annular TSVs with various inner diameters and a fixed outer diameter (D_f = 20 μm, ΔT = −250 ºC) [48].

4.5.2 Effect of dielectric liner

To incorporate TSVs in 3-D interconnects, coatings of barrier and/or dielectric materials may be needed between the TSV and Si. As discussed in Chapter 3, a compliant dielectric liner such as BCB (benzocyclobutene) can serve as a stress buffer to reduce the thermal stress in Si, thus reducing the area of KOZ. In this section, the effect of a compliant dielectric liner on the TSV delamination is investigated.

FEA simulations are performed to calculate the energy release rate for interfacial delamination between the dielectric liner and TSV. Here, Cu and BCB are chosen as the TSV and the dielectric material, respectively. The thickness of the dielectric liner ranges from 0.5μm to 2μm, while the diameter of Cu TSV is fixed at 20μm. A thermal load -250^{o}C is applied for FEA simulation. There are two interfaces in such kind of models: the Cu/BCB interface and the BCB/Si interface. Previous adhesion measurements have reported Γ= 12.2 J/m^2 for the Cu/BCB interface and Γ> 24 J/m^2 for the Si/BCB interface [53]. Therefore, an interfacial delamination between the Cu/BCB interface is assumed to take place for the following simulation.

Figure 4.9 plots the energy release rate versus the crack length for delamination along the Cu/BCB interface, in comparison to the Cu/Si interface without the BCB liner. When the crack is longer than 10μm, the ERRs among three lined structures are similar and all lower than the fully filled TSV. However, at a shorter crack length below 5μm, the ERRs of the lined TSVs can be higher than the fully filled TSV. This can be attributed to a larger out-of-plane displacement in the BCB liner near the wafer surface. Consider that the interfacial adhesion of BCB/Cu (12.2 J/m^2) is stronger than that of Si/Cu (9.0 J/m^2) and silicon oxide/Cu (3.8 J/m^2) [54]. Although the driving force for delamination is increased at a short crack length, the BCB liner is still beneficial to the TSV delamination problem.

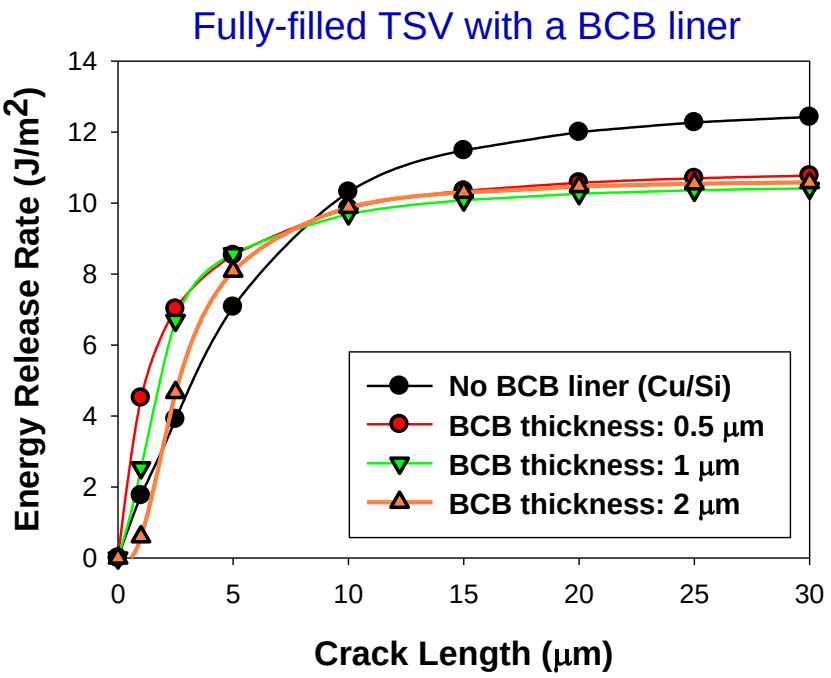
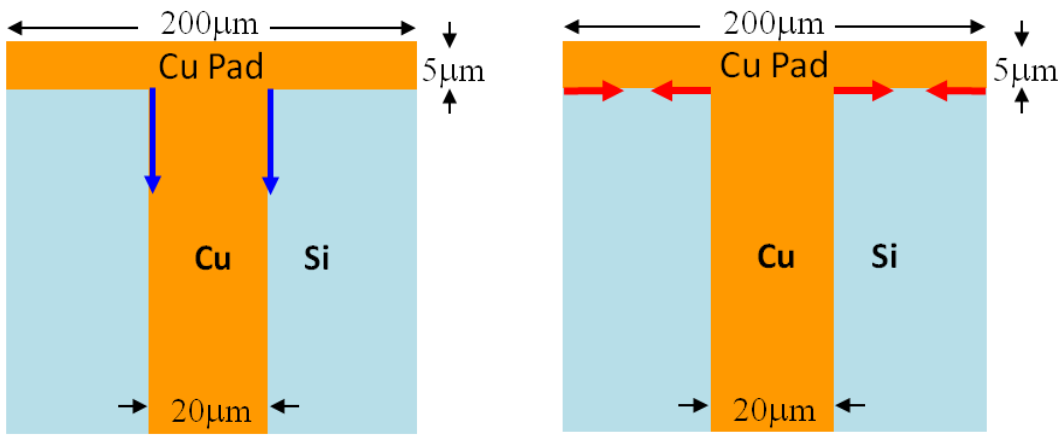


Figure 4.9: FEA-simulated ERRs for TSVs with a BCB liner. The fracture location is assumed to be the Cu/BCB interface (D_f = 20 μm, ΔT = −250 ºC) [49].

4.5.3 Effect of overlaying metal pad

After the metal filling process for TSVs, an additional metal layer is usually deposited on top of the TSVs. Such a metal layer can be photo-patterned to form landing pads for electrical connections. Consider a circumferential crack growing along the vertical TSV/Si interface (Figure 4.10a). The overlaying metal pad is expected to constrain the crack propagation along the vertical interface, and thus reduce the ERR for TSV delamination.



(a) Vertical, circumferential crack **(b) Horizontal, circumferential cracks**

Figure 4.10: Schematics of various interfacial crack geometries considered in a "nail head" TSV structure.

The TSV delamination under an overlaying metal pad was previously examined [18][26]. Consider a vertical, circumferential crack propagating downward underneath a rigid metal pad (Figure 4.10a). The delamination is mainly driven by a negative thermal load because the crack driving force generated by a positive thermal load was found to be one order of magnitude smaller [49]. An analytic solution for the crack driving force under a negative thermal load ΔT can be expressed as follows:

$$G_{SS} = \frac{E_m (\Delta\alpha\Delta T)^2 D_f}{4}\left(\frac{(1+\nu_f)^3(1-2\nu_f)(1-\alpha_D{}^2)+(1+\nu_m)(1+\nu_f)^2(1+\alpha_D)^2}{\left\langle (1+\nu_f)(1-2\nu_f)(1-\alpha_D)+(1+\nu_m)(1+\alpha_D)\right\rangle^2} \right), \quad (4.6)$$

By neglecting the elastic mismatch between the TSV and the matrix, Equation 4.6 can be simplified to become Equation 4.4. FEA simulations are performed to validate Equation 4.6. An axial-symmetric FEA model is built according to the geometry in Figure 4.10a, and the crack driving force was simulated as a function of the vertical crack length for a 20 μm Cu TSV under a -250°C thermal load. In Figure 4.11, the calculated ERR is plotted and compared with another 20 μm Cu TSV without the overlaying Cu pad. The results show a good agreement between the analytical solution and the FEA simulations for the steady-state case with a long crack length. The FEA simulation also indicates that an overlaying Cu pad with the thickness of a quarter of TSV diameter is rigid enough to restrict the crack opening and to reduce the ERR for TSV delamination by ~35%.

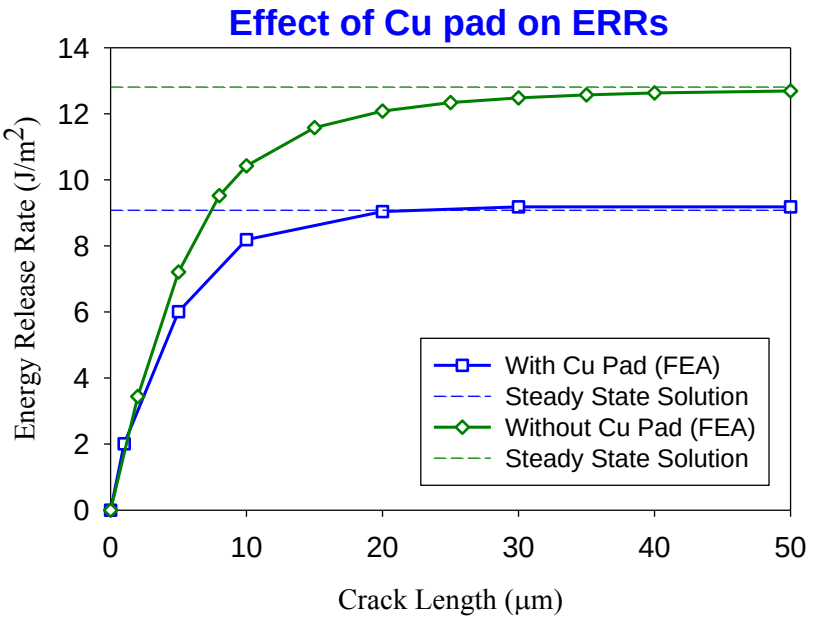


Figure 4.11: Effect of an overlaying Cu pad on ERR for delamination at the vertical interface (D_f = 20 μm, ΔT = −250 ºC) [49].

The overlaying metal pad can reduce the risk of TSV delamination, and the metallization process for TSVs can be engineered accordingly. For instance, an overburden of copper layer also comes with the electroplating process and has to be removed using a chemical-mechanical polishing (CMP) process after annealing. The copper overburden is rigid and can keep the TSV/matrix interfaces from delaminating. If the overburden is fully removed, the ERR for TSV delamination will increase by ~35% as mentioned earlier. Without the protection of the overlaying copper film, such TSV structure needs to go through another thermal process to form the metal contact on top, which can further increase the risk of delamination. Therefore, a metallization process that does not fully deplete the copper overburden is expected to reduce the risk of TSV delamination along the vertical TSV interface as discussed here.

4.6 PROTRUSION MECHANISM FOR NAIL-HEAD TSVS

During manufacturing of 3D-ICs, Si wafers containing TSVs are subjected to repeated thermal cycles between room temperature and the deposition temperature for BEOL structures (up to 400^{o}C). Interfacial cracks can develop along the via sidewall during cyclic thermal loadings. After extensive interfacial delamination, TSVs can expand in the axial direction without constraint under a positive thermal load. Consequently, TSV can protrude from the Si substrate and damage the overlaying structures. An example of such TSV protrusion phenomenon is shown in Figure 4.12 [17].

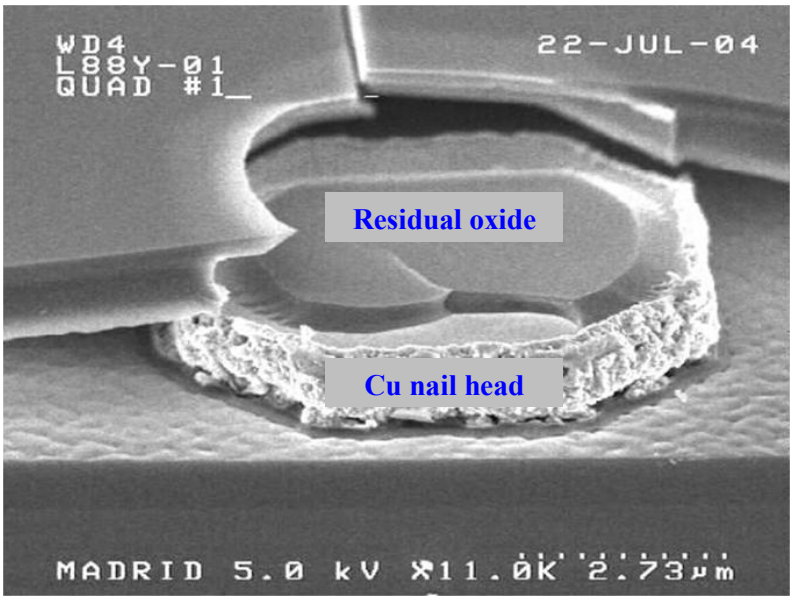


Figure 4.12: A Cu TSV protruded from the Si substrate and damaged the overlaying silicon oxide layer (Source: Tezzaron in Ref. [17])

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The Cu TSV in Figure 4.12 is similar to the nail-head structure illustrated in Figure 4.10. Before a nail-head TSV can protrude from the Si substrate, both the horizontal and the vertical TSV interfaces have to be delaminated. The energy release rate for cracking along the vertical interface has been calculated in the previous section. The energy release rate for the horizontal cracking is discussed in the following.

Consider a horizontal, circumferential cracking at the interface between the Si top surface and the flange part of the nail head (Figure 4.10b). As illustrated in Figure 4.10b, such interfacial cracking can propagate along two opposite directions. The crack can either: (a) initiate from the via edge and propagate to the outer-portion of the flange, or (b) initiate from the border of the flange and propagate toward the via. For scenario (a), the horizontal cracking is mainly driven by a positive thermal load. Under a positive

thermal load, the Cu via tends to extrude out of the Si substrate due to the larger thermal expansion of Cu, resulting in a tensile peeling stress at the horizontal interface. Such tensile stress can drive crack propagation from the inner- to the outer-portion of the flange. In contrast, under a negative thermal load, a compressive stress is induced at the horizontal interface, which does not contribute to the crack driving force. For scenario (b), the horizontal cracking can be driven by the shear stress at the border of the flange. The shear stresses are opposite in sign depending on whether a heating or a cooling thermal load. In both cases, the shear stress should drive the horizontal interfacial delamination with the same magnitude of ERR.

The energy release rate for the horizontal cracks is simulated using FEA. Based on the geometry in Figure 4.10b, two axial-symmetric FEA models are built for the crack driving force calculation for a +250^{o}C of thermal load. FEA simulations are performed separately for both the outward and the inward circumferential cracks, and the results are shown in Figure 4.13. For the outward crack, the ERR reaches a maximum at ~2 μm away from the edge of the TSV. As the crack tip extends away from the edge of the TSV, the crack driving force gradually decreases to zero. On the other hand, the ERR for the inward crack generally increases as the crack tip approaches the edge of the TSV. A comparison between the energy release rates in Figure 4.13 suggests that the horizontal cracking is more likely to initiate at the edge of Cu TSV and then grow outwards under a positive thermal load. Another comparison between Figure 4.11 and Figure 4.13 indicates that the energy release rate for a vertical crack under cooling is much larger than that for a horizontal crack under heating. The result suggests that the delamination is more likely to initiate from the vertical interface during repeated thermal cycles.

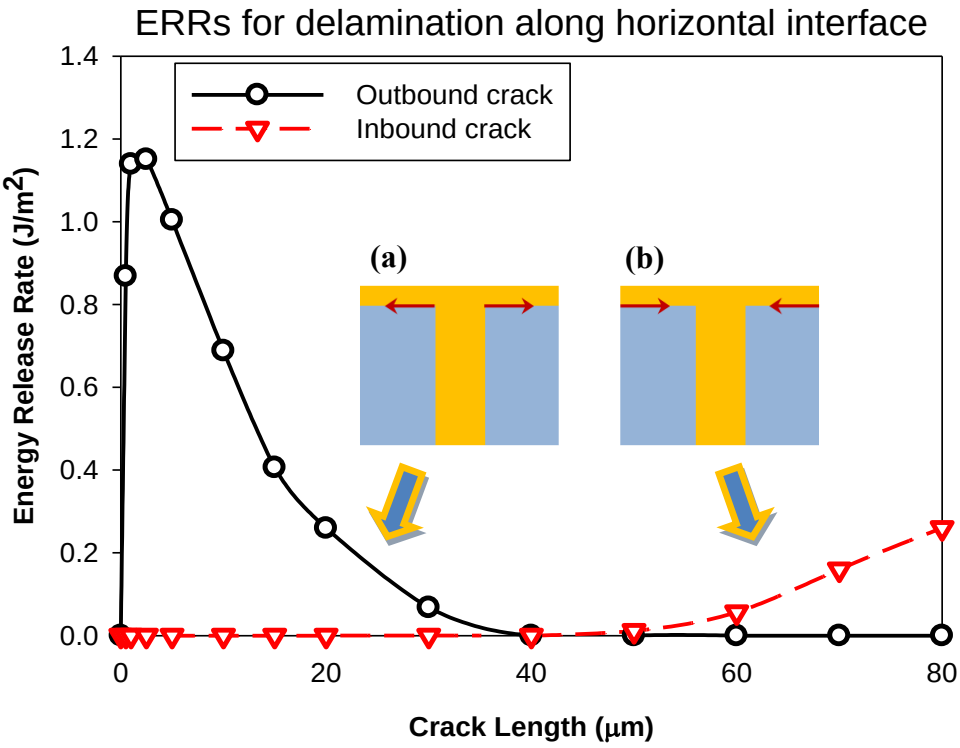

Figure 4.13: FEA-simulated ERRs for outbound and inbound crack along the Cu flange/Si interface (D_f = 20 μm, ΔT = +250 ºC) [49].

According to the previous analysis, a possible mechanism for TSV protrusion is proposed here. First, the vertical interface between the TSV and the silicon substrate is delaminated during negative thermal loadings. Once the vertical interface is debonded, the copper via is easier to protrude from the wafer upon heating, resulting in an increased crack driving force on the horizontal interface. After repeated thermal cycles, both vertical and horizontal interfaces can be sufficiently delaminated to induce the TSV protrusion from the Si wafer. This process is illustrated in Figure 4.14.

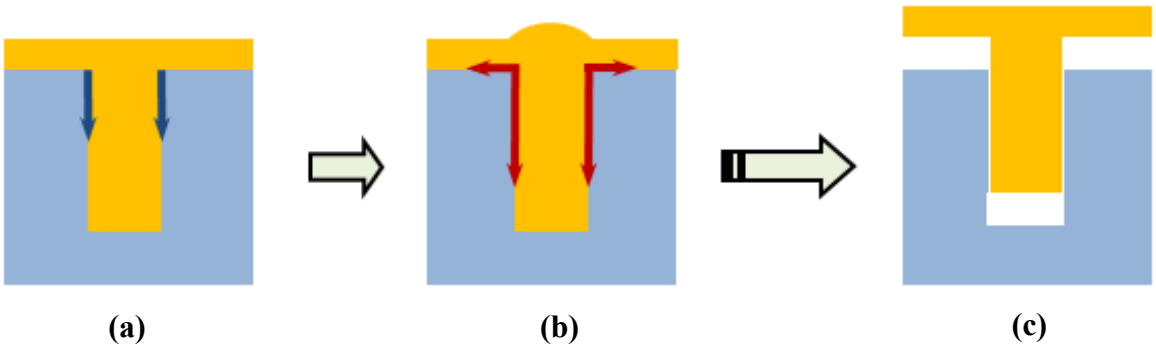

Figure 4.14: Illustration of TSV protrusion process: (a) Vertical interface debonding under cooling, (b) Horizontal interface debonding under heating, (c) TSV protrusion after repeated thermal cycles.

4.7 SUMMARY

In this chapter, the characteristics of thermal stress-induced TSV delamination have been investigated using analytical solutions and FEA simulations. The driving force for TSV delamination is found to be different depending on whether a positive or a negative thermal load. Under a positive thermal load, the fracture mode is primarily a shear mode (mode II) delamination. On the other hand, the fracture mode under a negative thermal load is a mixture of peeling (mode I) and shear (mode II).

According to the analytical solutions derived for a long crack at the steady state, it is found that reducing the TSV diameter and the thermal strain yield definite advantages in lowering the crack driving force for TSV delamination. FEA simulations further suggest that the crack driving force can be reduced by reducing the defect size (or crack length) and by thinning down the wafer thickness. The effect of metallization on TSV delamination is investigated using four materials: aluminum, copper, nickel and tungsten.

Tungsten exhibits the least ERR due to the smallest CTE mismatch with the silicon substrate. TSVs with various filling structures are compared. Annular structure exhibits lower ERRs than the fully filled TSV structure, and an overlaying metal pad can constrain the crack opening and thus reduce the ERR for delamination along the axial direction. Finally, a possible mechanism for TSV protrusion is proposed for a nail-head TSV structure. Interfacial cracking initiates at the vertical TSV/Si interface under cooling and then develops into the horizontal metal pad/Si interface under heating. TSV protrusion can occur after both TSV interfaces are delaminated from the Si matrix.

Chapter 5: Thermal Stress Interaction between TSVs and its Impact on Reliability

5.1 INTRODUCTION

To enable high density 3-D interconnects, groups of TSVs are required to be incorporated in array configurations. TSVs are not isolated from one another. Consequently, thermal, electrical, and thermo-mechanical interactions among adjacent TSVs are expected. For instance, the capacitive coupling in a TSV array has been found to increase with reducing the distance between TSVs [55]. A previous study by us indicates the thermal stresses can be intensified by reducing the lateral distance between TSVs [52]. With the ever increasing interconnect density, it is expected that the distance between TSVs will be reduced continuously in the future. Therefore, the effects of TSV proximity on the reliability of 3-D interconnects cannot be overlooked.

Previously, an isolated TSV structure has been examined in Chapter 3 and Chapter 4. In this chapter, the stress interaction in TSV arrays will be investigated. In Section 5.2, the thermal stress interaction between TSVs will be deduced based on linear superposition of a 2-D plane-strain stress solution. Due to the elastic interaction, thermal stress components are found to be intensified or suppressed in the space between TSVs. The stress analysis is further extended in Section 5.3 to study the keep-out zone (KOZ) for MOS devices in a TSV array. In the last, Section 5.4, a potential Si cracking behavior is introduced, and the effect of TSV proximity on the crack driving force will be examined.

5.2 THERMAL STRESS INTERACTION BETWEEN TSVS

The characteristics of thermal stress interaction between TSVs are discussed in this section. For simplicity, the stresses are based on the 2-D plane-strain solution. For the discussion of the KOZ in the MOS devices, knowledge of near-surface stresses is required, which will be simulated using FEA in the next section.

The 2-D plane-strain solution for an isolated TSV has been presented previously in Section 3.2. The stress components are linearly superposable in a Cartesian coordinate system. Therefore, the solution in the Cartesian system (Equation 3.6) is applied here. Consider an infinite Si substrate containing multiple TSVs, with their centers located at (x_i, y_i). Ignoring the elastic mismatch between TSVs and the Si substrate, the thermal stresses in Si can be expressed as:

$$\sigma^{Si}{}_{xx} = -\sigma^{Si}{}_{yy} = -\frac{E\varepsilon_T {D_f}^2}{8(1-\nu)} \sum_i \frac{(x-x_i)^2-(y-y_i)^2}{\left[(x-x_i)^2+(y-y_i)^2\right]^2}$$
$$\sigma^{Si}{}_{xy} = -\frac{E\varepsilon_T {D_f}^2}{4(1-\nu)} \sum_i \frac{(x-x_i)(y-y_i)}{\left[(x-x_i)^2+(y-y_i)^2\right]^2} \quad , \tag{5.1}$$

and the thermal stresses inside a TSV with its center located at (x_j, y_j):

$$\sigma^{TSV}{}_{xx} = -\frac{E\varepsilon_T {D_f}^2}{8(1-\nu)} \left\{ \sum_i \frac{(x-x_i)^2-(y-y_i)^2}{\left[(x-x_i)^2+(y-y_i)^2\right]^2} - \frac{(x-x_j)^2-(y-y_j)^2}{\left[(x-x_j)^2+(y-y_j)^2\right]^2} + \frac{4}{{D_f}^2} \right\}$$
$$\sigma^{TSV}{}_{yy} = \frac{E\varepsilon_T {D_f}^2}{8(1-\nu)} \left\{ \sum_i \frac{(x-x_i)^2-(y-y_i)^2}{\left[(x-x_i)^2+(y-y_i)^2\right]^2} - \frac{(x-x_j)^2-(y-y_j)^2}{\left[(x-x_j)^2+(y-y_j)^2\right]^2} - \frac{4}{{D_f}^2} \right\} \quad , \tag{5.2}$$
$$\sigma^{TSV}{}_{xy} = -\frac{E\varepsilon_T {D_f}^2}{4(1-\nu)} \left\{ \sum_i \frac{(x-x_i)(y-y_i)}{\left[(x-x_i)^2+(y-y_i)^2\right]^2} - \frac{(x-x_j)(y-y_j)}{\left[(x-x_j)^2+(y-y_j)^2\right]^2} \right\}$$

Based on Equation 5.1 and 5.2, the thermal stress distribution in a TSV array can be developed. An example of the stress interaction between two TSVs is given below. Consider two TSVs aligned along the *y* axis under an arbitrary thermal load. The diameter of both TSVs is 20 μm, and the distance between the centers of two TSVs is 40 μm. The distribution of thermal stresses in such bi-TSV system can be obtained by plotting Equation 5.1 and 5.2 using the MATLAB® software (Figure 5.1):

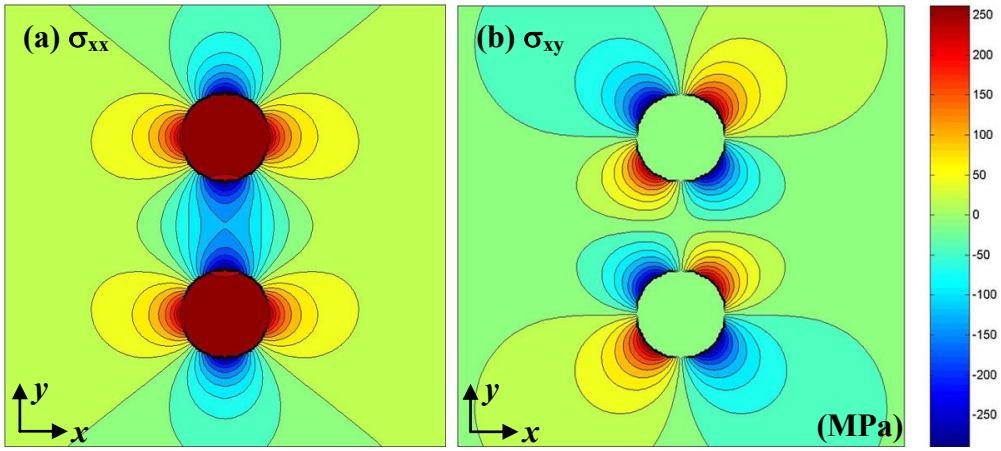

Figure 5.1: Thermal stresses induced by two TSVs aligned along the y axis: (a) Distribution of normal stress σ_{xx}; (b) Distribution of shear stress σ_{xy}.

Comparing to the stress field induced by an isolated TSV (Figure 3.5), the two-fold rotational symmetry is broken due to the elastic interaction between two TSVs. In Figure 5.1a, the normal stress σ_{xx} is intensified in the space between two TSVs. On the other hand, the shear stress σ_{xy} is suppressed in the same area (Figure 5.1b). As discussed in Chapter 3, the KOZ for MOS devices is mainly controlled by the magnitude of the normal stresses instead of the shear stress. As a result, the area of KOZ may be increased in the space between two adjacent TSVs.

Another example given below demonstrates a distinct effect of the stress interaction. Consider two TSVs aligned along the [1,1] coordinate direction. The TSV diameter, pitch distance, and thermal loading are remained the same as in the previous example. The thermal stress distribution in such bi-TSV system is plotted in Figure 5.2.

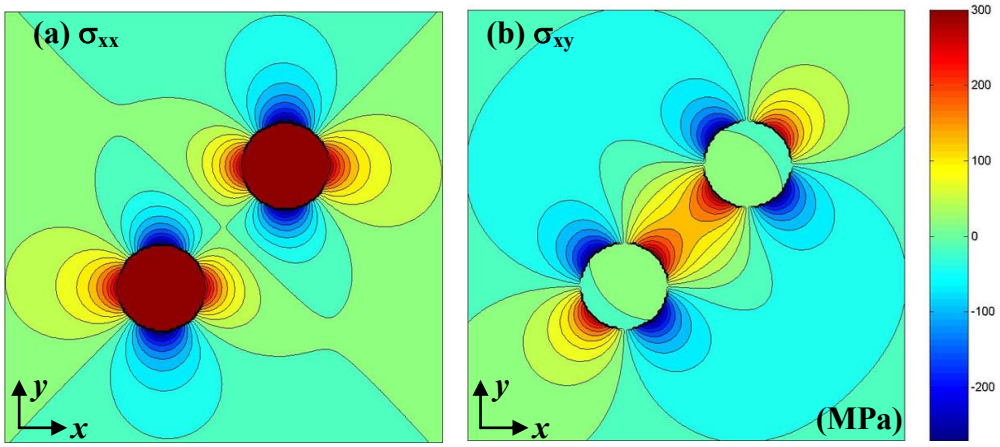

Figure 5.2**:** Thermal stresses induced by two TSVs aligned along [1,1] coordinate direction: (a) Distribution of normal stress σ_{xx}; (b) Distribution of shear stress σ_{xy}.

In Figure 5.2, it is clear that the normal stress σ_{xx} is suppressed in the space between two adjacent TSVs while the shear stress σ_{xy} is intensified in the same area. It implies the area of KOZ may be reduced in the space between two TSVs. Based on these two examples, the interaction of a specific stress component depends on how the TSV array is arranged, and the arrangement of TSV array may impact the KOZ design. This interesting subject will be further examined in Section 5.3.

The other observation in the bi-TSV system is the existence of two stress-free points in the Si substrate as a result of destructive stress interaction. Figure 5.3 shows the distribution of von Mises stress for aforementioned two examples with (a) TSVs aligned along y axis and (b) TSVs aligned along [1,1] direction. Imagine that two TSVs are

located at the diagonal corners of a square, the other two corners of the square come out as the stress-free points. At stress-free points, the radial stress from one TSV is canceled by the circumferential stress from the other TSV, with all other stress components being zero. Under the plane-strain condition, such stress-free points exist regardless of the array orientation, the TSV diameter, and the distance between TSVs.

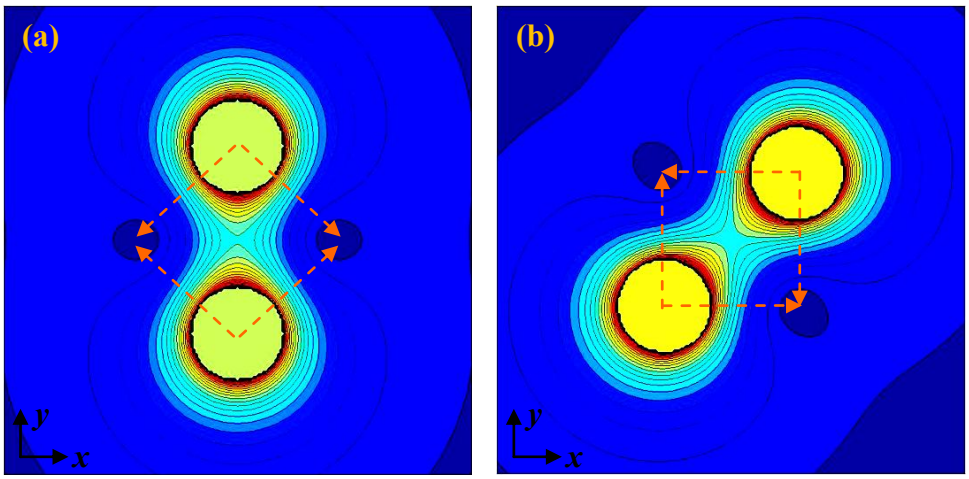

Figure 5.3: Distribution of von Mises stress showing two stress-free points in the Si matrix as a result of destructive stress interaction: (a) TSVs aligned along y axis; (b) TSVs aligned along [1,1] coordinate direction.

5.3 Effect of Stress Interaction on KOZ

In this section, the near-surface thermal stresses in bi-TSV systems are first simulated using FEA, which is followed by the KOZ calculation for bi-TSV structures with various spacing distances. A 3-D FEA model containing one-eighth of a bi-TSV structure is constructed in ANSYS® software, as illustrated in Figure 5.4. Symmetric boundary conditions are applied on the surfaces at x = 0, y = 0, and z = 0 so that such FEA model is equivalent to a bi-TSV system. A 3-D solid element (SOLID185) in the

ANSYS® software is selected for simulations. The TSV diameter D_f is 20 μm and the wafer thickness H is 100 μm. The distance between two TSVs, p, ranges from $2D_f$ to $5D_f$. The TSV material is taken to be Cu. The material properties for FEA simulation is listed in Table 5.1. For simplicity, the elastic anisotropy of Cu and Si is ignored.

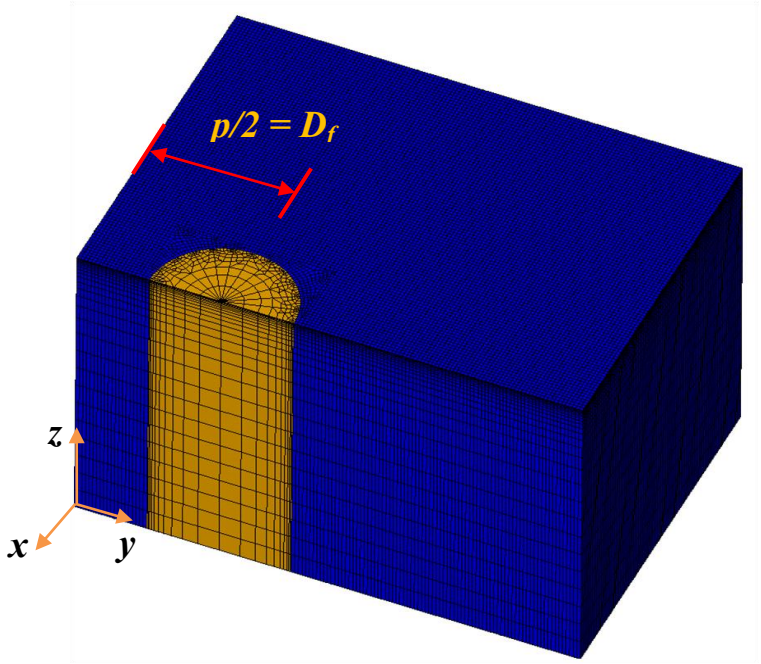

Figure 5.4**:** Element mesh in a one-eighth FEA model. Symmetry boundary conditions are applied at x = 0, y = 0, and z = 0 in order to simulate the bi-TSV system.

Table 5.1: Thermo-mechanical properties of the materials for FE stress analysis [27-28]

Material	CTE (ppm/K)	Young's Modulus (GPa)	Poisson's ratio
Si	2.3	130	0.28
Cu	17	110	0.35

After constructing the FEA model, a negative thermal load $\Delta T = -180^{o}C$ is applied for stress simulation. Then, the simulation results are used to calculate the stress-induced mobility change in MOSFET devices using Equation 3.9. Because the devices are located very near the top Si surface, the stress results on the top wafer surface are taken for the calculation. The device considered here is p-MOSFET on a (001) Si substrate with its channel along [110] direction. The mobility change are calculated for following two cases: (A) two TSVs aligned along [110] direction, and (B) two TSVs aligned along [100] direction.

Figure 5.5 shows the contour plot of mobility change for case (A). Here the effect of TSV proximity is observed by comparing two bi-TSV systems of different pitch ($p = 3D_f$ vs. $p = 5D_f$). In Figure 5.5, the outermost black lines depict the contour for 10% mobility change. If two TSVs are far away from each other (Figure 5.5b, $p = 5D_f$), the mobility contours remain unaffected. If distance between two TSVs is shorter (Figure 5.5a, $p = 3D_f$), the area with a mobility change > 10% is increased in the space between two TSVs. Consequently, the KOZ for p-MOSFET// [110] is increased by the proximity of two TSVs..

Figure 5.6 shows the contour plot of mobility change for case (B), where two TSVs are aligned along [100] direction. The distance between two TSVs is $3D_f$ and $5D_f$ in Figure 5.6a and 5.6b, respectively. Comparing Figure 5.6a to 5.6b, the area with a mobility change > 10% is slightly reduced when two TSVs are close to each other. Therefore, the proximity of two TSVs will slightly reduce the KOZ. Based on the observation from case (A) and (B), it is clear that the effect of TSV proximity depends on how the TSV array is arranged. It is possible to minimize the KOZ by properly positioning the TSVs.

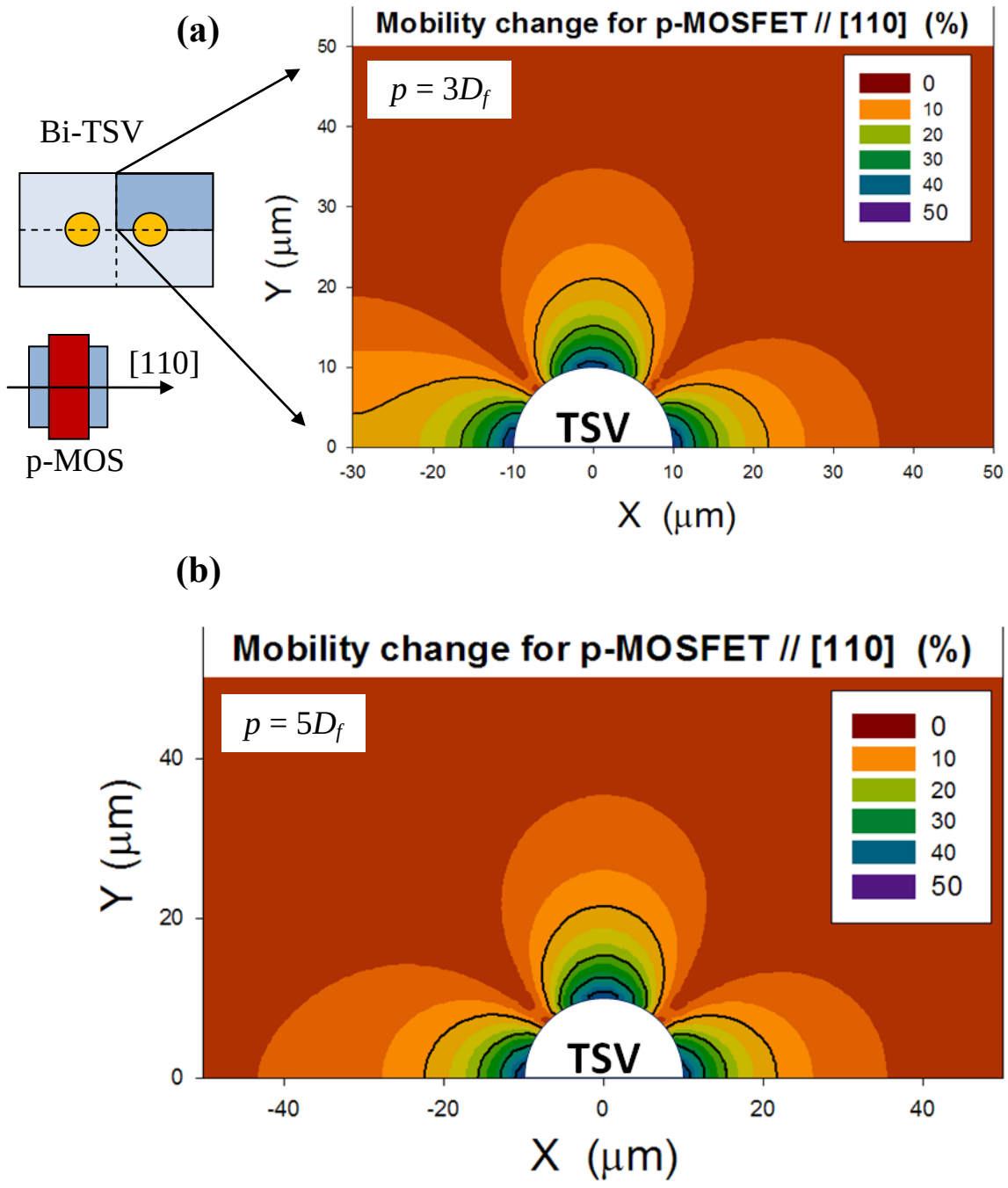

Figure 5.5: Contour plots of mobility change in p-MOSFET // [110] direction. Two TSVs are aligned along [110] direction. (a) Distance between two TSVs is 60 μm; (b) Distance between two TSVs is 100 μm.

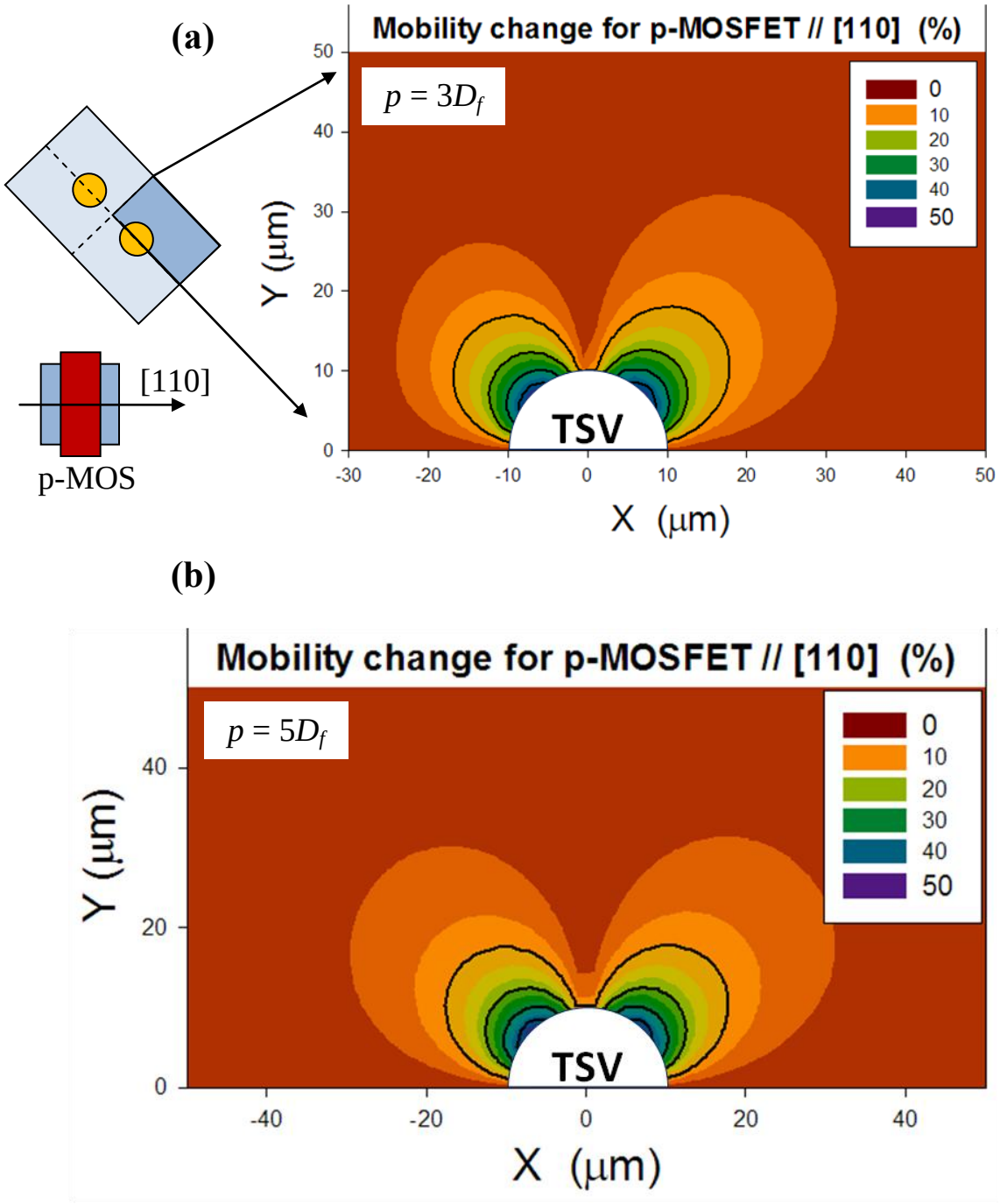

Figure 5.6**:** Contour plots of mobility change in p-MOSFET // [110] direction. Two TSVs are aligned along [100] direction. (a) Distance between two TSVs is 60 μm; (b) Distance between two TSVs is 100 μm.

Finally, the KOZ is defined to be the area with a mobility change greater than 10%, and the total area of KOZ surrounding such bi-TSV structure is calculated. Figure 5.7 shows the comparison among bi-TSV systems of various spacing distance ($2D_f$, $3D_f$, $4D_f$, $5D_f$) and of different alignment directions ([100], [110]).

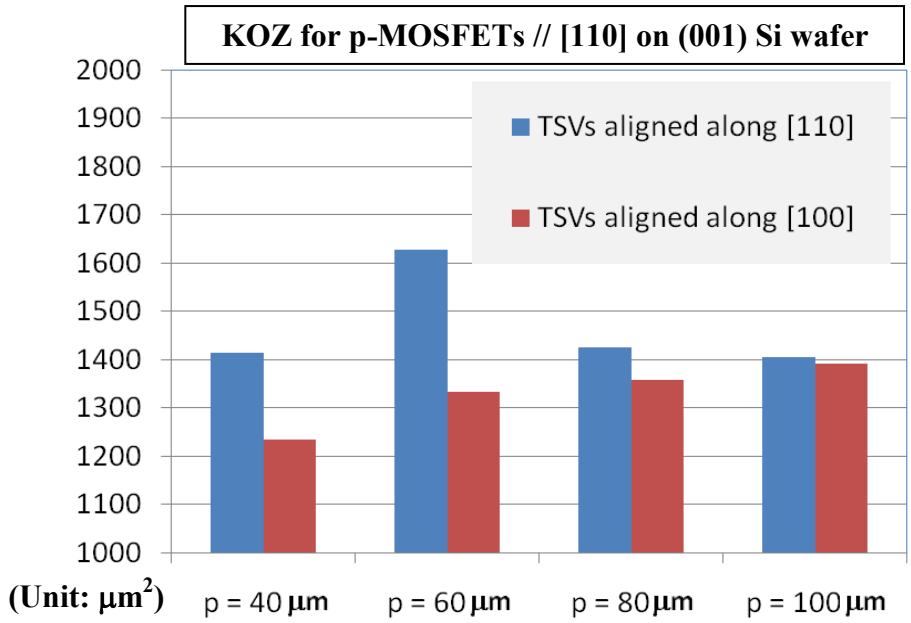

Figure 5.7: Comparison on the area of KOZ (mobility change > 10%) among various bi-TSV structures. (D_f = 20 μm, ΔT = −180 ºC)

In Figure 5.7, the KOZ reduces monotonically when two TSVs approach each other along the [100] direction. This is attributed to a destructive stress interaction in the space between two TSVs. When two TSVs approach each other along the [110] direction, the KOZ initially increases due to the constructive stress interaction, and reaches a maximum at a distance ~$3D_f$. If the distance is further reduced to 2 D_f, the KOZ in the space between two TSVs would overlap with each other, resulting in a reduction in the

total area of KOZ. In short, the proximity of two TSVs affects the area of KOZ. Depending on the alignment direction, the total KOZ can be increased by 16% or be reduced by 12% in this study.

5.4 EFFECT OF TSV PROXIMITY ON SI CRACKING

This section discusses the thermal stress-induced Si cracking, another potential failure mode in TSV structures. The Si cracking induced by an isolated TSV is first discussed in Section 5.4.1. In Section 5.4.2, the TSV proximity effect on Si cracking is studied in a bi-TSV structure.

5.4.1 Crack driving force for Si cracking: isolated TSV

TSV-induced thermal stresses can drive Si cracking under a positive thermal load. Because the CTEs of metallic materials for TSV are larger than that of Si, TSVs expand more than the Si matrix under heating. Consequently, a tensile circumferential stress $\sigma_{\theta\theta}$ builds up in the Si matrix. Such tensile stress can drive a through-thickness crack on the edge of TSV to propagate into the Si matrix along the radial direction, as illustrated in Figure 5.8a. An analogous fracture behavior, matrix cracking in fiber-reinforced composites, has been observed and well studied before (Figure 5.8b, [56]). This section uses a similar approach to investigate the driving force for Si matrix cracking in TSV interconnects.

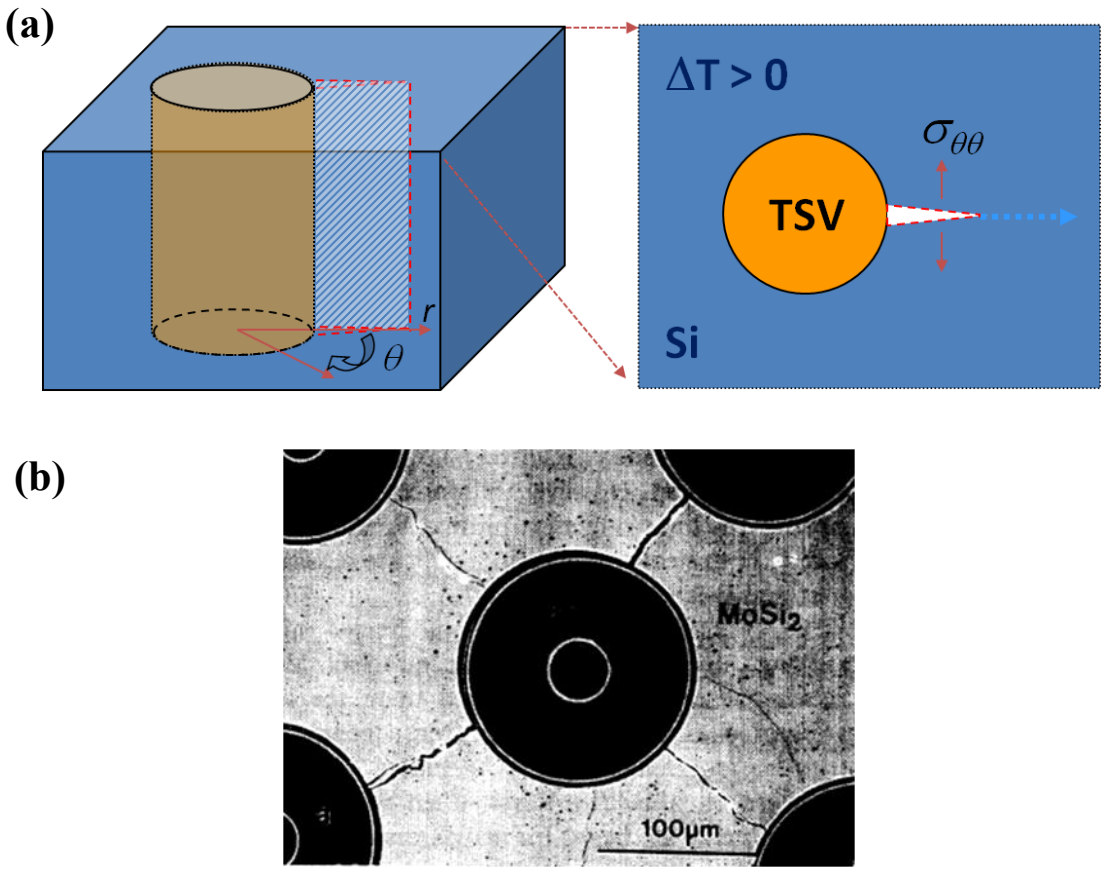

Figure 5.8: (a) Illustration of TSV-induced Si cracking under a positive thermal load; (b) Matrix cracking behavior observed in a SiC fiber-reinforced $MoSi_2$ composite. (Source: Lu et al. in Ref. [56])

The crack driving force for the matrix cracking was derived by Suo [57] and was further developed by Lu [56]. Consider an infinitely long fiber embedded in an infinite matrix, with a pre-existing through-thickness crack located near the fiber (Figure 5.9). Given a positive thermal load ΔT, the mode-I stress intensity factor K_I and the energy release rate G_I can be expressed as [56]:

$$K_I = \frac{D_f{}^2 E \Delta\alpha \Delta T}{4(1-\nu)} \sqrt{\frac{\pi a}{8 d_1 d_2{}^3}} \cos\left(\frac{\theta_1}{2} + \frac{3\theta_2}{2}\right), \tag{5.3}$$

$$G_I = \frac{K_I{}^2 (1-\nu^2)}{E}, \tag{5.4}$$

Where a is the length of the through-thickness crack. The elastic mismatch between the fiber and the matrix is ignored for simplicity. The distance and angular direction between the fiber and the through crack (d_1, d_2, θ_1, θ_2) are defined in Figure 5.9:

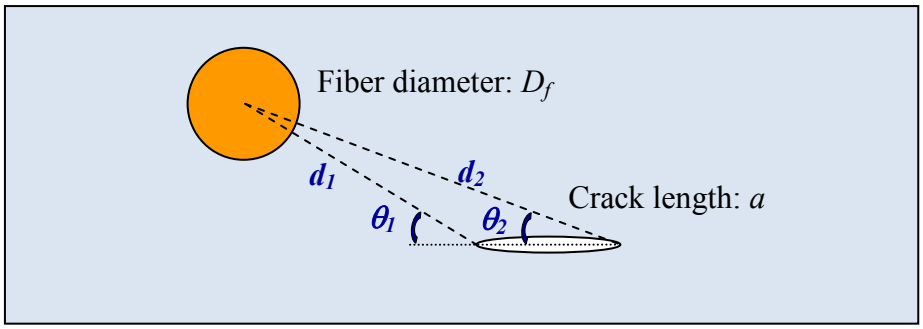

Figure 5.9: Cross-section view of a fiber along with a through crack embedded in an infinite matrix. (Source: Lu et al. in Ref. [56]. The diagram is redrawn by the author)

The driving force for TSV-induced Si cracking can be obtained from Equation 5.3 and 5.4. Consider a through-thickness crack extending from the edge of a Cu TSV subjected to a positive thermal load $\Delta T = +250^{o}C$ (Figure 5.8a). The energy release rate G_I is plotted as a function of the crack length in Figure 5.10.

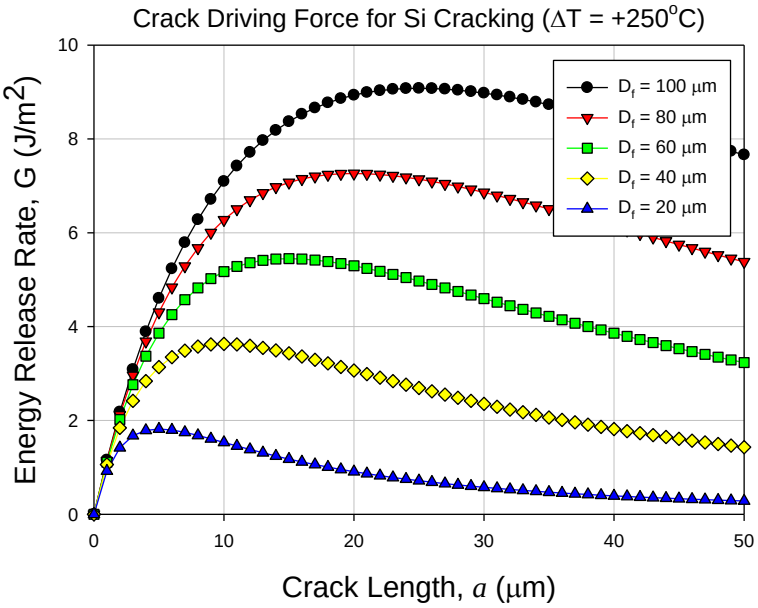

Figure 5.10: Energy release rate for TSV-induced Si cracking. ($\Delta T = +250^{o}C$)

In Figure 5.10, the driving force for TSV-induced Si cracking generally increases with the TSV diameter. The driving force initially increases with the crack length, and then gradually reduces at a crack length $a > D_f/4$. This is due to the reason that the circumferential stress acting on the crack tip decreases exponentially as the crack tip moves far away from the TSV. Given the cohesive fracture energy of Si (5 ~ 6 J/m^2), the TSV-induced Si cracking may not occur if a TSV diameter is below 60 μm under a thermal load +250^{o}C. Si cracking can be induced by a relatively large size of TSV with a long pre-crack (e.g. D_f = 100 μm, a > 5 μm).

5.4.2 Crack driving force for Si cracking: bi-TSV

The proximity of TSVs can either intensify or reduce the thermal stresses in Si. As a result, the driving force for Si cracking can be affected by the arrangement of TSVs. In this section, the effect of TSV proximity on Si cracking is examined using a bi-TSV structure. Here two cases are considered: (A) Cracking direction is parallel to the alignment direction of two TSVs, and (B) Cracking direction is perpendicular to the alignment direction of two TSVs. These two cases are illustrated in Figure 5.11. In the following calculation, Cu is chosen to be the TSV material, and the diameter of both TSVs is 100 μm. The distance p between two TSVs ranges from $2D_f$ to $5D_f$. A positive thermal load $\Delta T = +250^{o}C$ is applied.

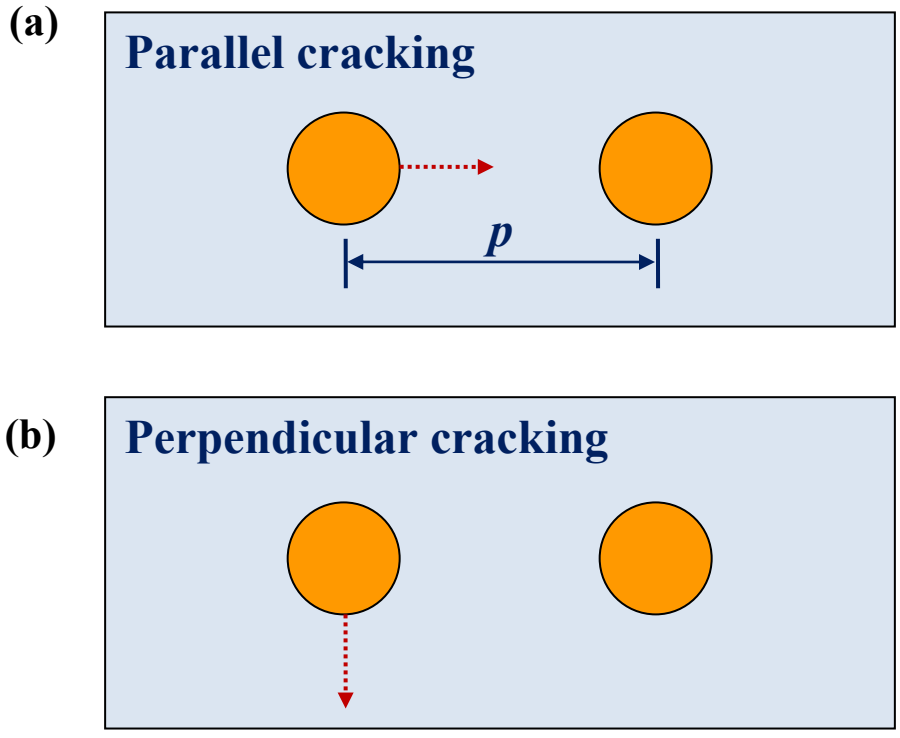

Figure 5.11: (a) Si cracking direction is parallel to the alignment of TSVs; (b) Si cracking direction is perpendicular to the alignment of TSVs.

For case (A) and (B), Equation 5.3 is used to calculate the mode-I stress intensity factor (K_I). Because the mode-I stress intensity factor is linearly superposable, the effective K_I in the bi-TSV structure is simply the summation of that contributed by each TSV. Once the total K_I is determined, the total energy release rate, G, can be derived using Equation 5.4.

The energy release rate for case (A), a parallel Si cracking, is plotted as a function of the crack length in Figure 5.12. The driving force for Si cracking is significantly increased with $p = 2D_f$. This is due to a constructive interaction on the circumferential stress between two TSVs. With a distance p farther than $3D_f$, however, the proximity effect is minimum.

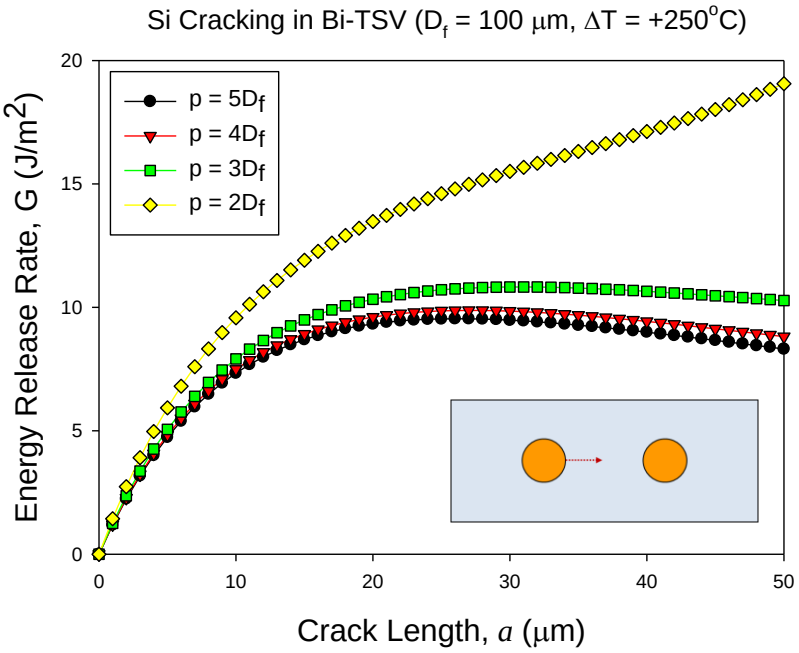

Figure 5.12: TSV proximity effect on the driving force for Si cracking: case (A).

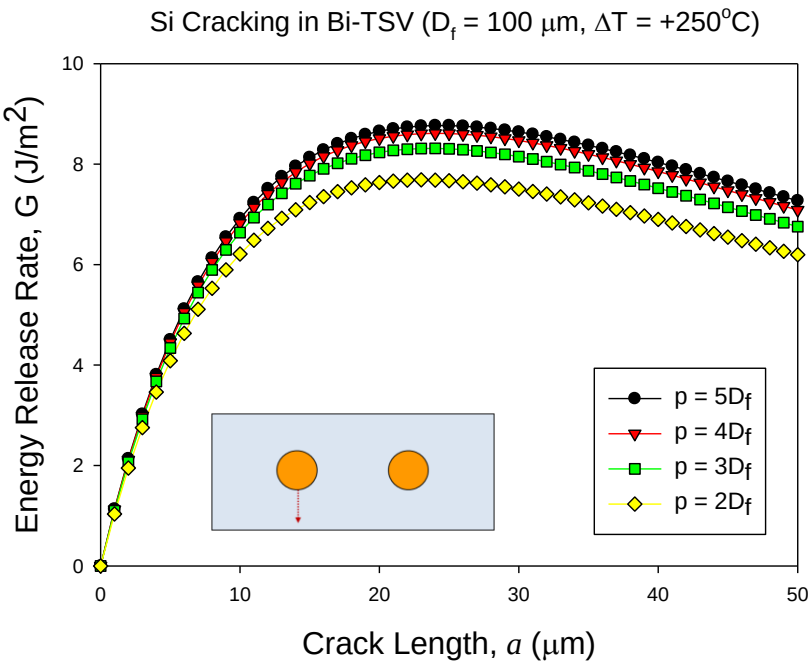

Figure 5.13: TSV proximity effect on the driving force for Si cracking: case (B).

Figure 5.13 plots the energy release rate for case (B), where the Si cracking direction is perpendicular to the alignment of TSVs. The crack driving force slightly decreases with a decreasing distance between two TSVs. This is attributed to the fact that the circumferential stress (or opening stress) on the crack tip is slightly reduced by the compressive radial stress field of the other TSV.

The pre-existing crack discussed in this section can be introduced during the Si drilling process. The direction of such edge cracks may be randomly distributed, creating an isotropic crack driving force in all directions for an isolated TSV. If two TSVs are close to each other, the driving force for Si cracking is intensified along the parallel direction (case (A)), but is slightly decreased along the perpendicular direction (case (B)). In addition, the fracture toughness is identical for Si cracking in cases (A) and

(B) due to the four-fold rotational symmetry of a (001) Si wafer. Consequently, the Si cracking propagates preferentially along the TSV alignment direction.

5.5 SUMMARY

The thermal stress interaction in a bi-TSV structure is investigated. Depending on the spacing distance and the alignment direction of two TSVs, the stress components can be intensified or be reduced in the Si matrix. As a result, the KOZ area as well as the driving force for Si cracking can be controlled to some degree by the spatial arrangement of two TSVs.

Specifically, in Section 5.3, the proximity of two TSVs along [110] direction increases the KOZ, while the proximity along [100] direction reduces the KOZ. In Section 5.4, the proximity of two TSVs parallel to the matrix cracking direction increases the crack driving force, while the proximity perpendicular to the cracking direction slightly reduces the crack driving force. These studies establish a basis for one to understand the thermo-mechanical interaction in a more complicated array structure. In short, it is possible to improve the thermo-mechanical reliability of 3-D interconnects by properly arranging the location of TSVs.

Chapter 6: Conclusions and Future Work

6.1 CONCLUSIONS

Models and simulations were established to explore the thermo-mechanical reliability in 3-D interconnects containing TSVs. The analysis consisted of four components: (1) a thermal stress measurement on TSV arrays combining the Bending Beam technique and FEA simulations, (2) a study of TSV-induced thermal stresses in Si matrix and the impact on electrical performance of MOSFET devices, (3) a study of TSV-induced thermal stresses at the TSV/Si interface and the resulting delamination problems, and (4) a study of the stress interaction in bi-TSV systems.

The bending beam technique measured the averaged bending curvature induced by the thermal expansion of a periodic annular Cu TSV array. The structural complexity of the blind annular TSV necessitated the use of FEA to derive the TSV-induced thermal stresses which accounts for the beam bending during thermal cycles. The FEA simulations established linear relationships between bending curvature and stress components in TSVs. Such linear relationships were used to extract independent stress components from the bending beam measurements. The results provided an understanding to the temperature dependent stress characteristics in TSVs.

TSV-induced stresses in Si were investigated combining analytical solutions and FEA simulations. In the Si matrix, TSV-induced radial and circumferential stresses were proportional to the thermal load, CTE mismatch between TSV and Si, and the square of the ratio between TSV diameter and the radial distance. The distribution of TSV-induced stresses was investigated in the Cartesian coordinate system for the KOZ study. In contrast to the axi-symmetrical distribution in the cylindrical coordinate system, a two-fold rotational symmetric stress distribution was found. Such two-fold symmetry provided an insight into the design for KOZ. FEA simulations were carried out to

calculate the area of KOZ surrounding isolated TSVs. It was found that the area of KOZ for MOSFETs is mainly decided by the device orientation as a result of anisotropic piezoresistivity effect. Parameter studies also suggested that the KOZ can be reduced by: (1) smaller TSV diameter, (2) thinner wafer thickness, (3) compliant dielectric liner, (4) low CTE metallic material, and (5) an annular structural design.

TSV-induced stresses at the TSV/Si interface were investigated, and the resulting driving force for TSV delamination was calculated. FEA simulations revealed a shear stress concentration at the circumference of TSV which accounts for the interfacial delamination. TSV delamination can also be driven by the tensile radial stress at the TSV/Si interface under cooling. Consequently, TSV interfaces are more prone to cracking under cooling processes. Similar to the analysis on KOZ, the delamination driving force can be reduced by a smaller TSV diameter, a thinner wafer thickness, and a smaller thermal loading. The selections of materials and the structural designs also impacted the magnitude of the driving force. Based on the analyses on delamination driving force, a TSV protrusion mechanism was proposed.

Finally, the effect of thermal stress interaction between adjacent TSVs has been studied for a bi-TSV structure. In the Cartesian coordinate system, the stress interaction can be either constructive or destructive, depending on how two TSVs are orientated. The stress interaction between two TSVs impacted the KOZ as well as the crack driving force for Si cracking. The proximity of two TSVs can have opposite effects on the area of KOZ depending on whether two TSVs are aligned along [110] or [100] direction. For Si cracking under a positive thermal load, the proximity of two TSVs can either increase or decrease the driving force, depending on whether a parallel or perpendicular cracking direction. The study points to the fact that the arrangement of TSV array can be engineered to improve the thermo-mechanical reliability of the 3-D interconnect.

6.2 FUTURE WORK

Analytical solutions for Bending Beam Measurement:

In the bending beam measurements, FEA simulations were performed to derive the thermal stresses from the bending curvature measured. As an alternative way, such stress analyses may be carried out by analytical solutions. Due to the structural complexity of the TSV structures, further development is required for the analytical solutions.

Local stress measurements using micro-Raman:

In the bending beam experiments, the bending is an averaged effect of the thermal expansion of a large population of vias. Although the stress components in Si/Cu vias can be derived using FEA simulations, the local stresses in the vias can vary with the local Cu thickness, the local oxide thickness, the elastic anisotropy in Cu grains, etc. Micro-Raman, which measures individual vias at room temperature, may be used to obtain a more precise measurement on the local stresses. The statistical result from Raman measurements can be further compared with that measured using the bending beam technique.

Shape effect on the driving force for TSV delamination:

The driving force for TSV delamination has been derived for axi-symmetric TSV structures. For non-axisymmetric TSVs such as an oval or a rectangular TSV, the driving force for TSV delamination can be very different. Specifically, an oval (or rectangular) TSV has a larger surface-to-volume ratio than that of a circular TSV. Conceptually, more elastic energy is required to drive an interfacial crack growth in a TSV structure with a

larger surface-to-volume ratio. However, the stress concentration may occur at the sharp corners of oval/rectangular TSVs, which may induce other reliability concerns. Such a study can be performed by doing fracture analyses in a 3-D FEA model.

TSV proximity effect on TSV delamination:

For the case of an isolated TSV, the TSV delamination is mainly driven by the shear stress concentration at the circumference of TSV. Whether the proximity of TSVs can reduce such shear stress concentration to improve the reliability is of interest. Similarly, such a study can be performed by doing fracture analyses in a 3-D FEA model.

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